ELectronics EXpress

IEICE Electronics Express, Vol.7, No.24, 1790–1795

# Floating body CMOS phototransistor memory

**Koichiro Kishima**[1a)], **Nick K. Hon**[2], **and Bahram Jalali**[2]

[1] *Core Device Development Group, Sony Corporation,*
*1–11–1 Osaki Shinagawa-ku, Tokyo, 141–0032 Japan*

[2] *University of California, Los Angeles,*
*Los Angeles, CA 90095–1594, USA*

a) *Koichiro.Kishima@jp.sony.com*

**Abstract:** An optoelectronic CMOS memory technology is proposed where photon induced floating body effect stimulates switching and hysteresis in the transistor. The floating body effect is induced by exceedingly few carriers generated by two photon absorption. In this paper we present the structure of proposing device and numerically validated the device by Atlas device simulator from SILVACO Corporation.

**Keywords:** detectors, optical memories, integrated optics

**Classification:** Optoelectronics, Lasers and quantum electronics, Ultrafast optics, Silicon photonics, Planar lightwave circuits

## References

[1] H. K. Tsang, C. W. Wong, T. K. Lang, I. E. Day, S. W. Robert, A. Harpin, J. Drake, and M. Asghari, "Optical dispersion, two-photon absorption and self-phase modulation in silicon waveguides at 1.5 $\mu$m wavelength," *Appl. Phy. Lett.*, vol. 80, no. 3, pp. 416–418, 2002.

[2] R. Salem, G. E. Tudury, T. U. Horton, G. M. Carter, and T. E. Murphy, "Polarization-Insensitive Optical Clock Recovery at 80 Gb/s Using a Silicon Photodiode," *Photon. Technol. Lett.*, vol. 17, pp. 1968–1970, 2005.

[3] E. Tien, N. S. Yuksek, F. Qian, and O. Boyraz, "Pulse compression and modelocking by using TPA in silicon waveguides," *Opt. Express*, vol. 15, no. 10, pp. 6500–6506, 2007.

[4] S. Okhonin, M. Nagoya, J. M. Sallese, and P. Fazan, "A SOI Capacitorless 1T-DRAM Concept," *Proc. 2001 IEEE Int. Conf.*, vol. 153, 2001.

[5] A. Singh, M. Ciraula, D. Weiss, J. Wuu, P. Bauser, P. de Champs, H. Daghighian, D. Fisch, P. Graber, and M. Bron, "A 2ns-Read-Latency 4 Mb Embedded Floating-Body memory Macro in 45 nm SOI Technology," *Proc. 2009 ISSCC*, vol. 460, 2009.

[6] D. Dimitropoulos, S. Fathpour, and B. Jalali, "Limitations of active carrier removal in silicon Raman amplifiers and lasers," *Appl. Phy. Lett.*, vol. 87, p. 261108, 2005.

[7] O. Boyraz and B. Jalali, "Demonstration of directly modulated silicon Raman laser," *Opt. Express*, vol. 13, no. 3, pp. 796–800, 2005.

[8] Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, "Micrometre-scale silicon electro-optic modulator," *Nature*, vol. 435, no. 19, pp. 325–327, 2005.

[9] K. Yamada, T. Tsuchizawa, T. Watanabe, J. Takahashi, H. Fukuda, M. Takahashi, T. Shoji, S. Uchiyama, E. Tamechika, S. Itabashi, and H.


DOI: 10.1587/elex.7.1790
Received November 07, 2010
Accepted November 16, 2010
Published December 25, 2010

Morita, "Silicon Wire Waveguiding System: Fundamental Characteristics and Applications," *Electronics and Communications in Japan, Part 2*, vol. 89, no. 3, pp. 42–55, 2006.

## 1 Introduction

Silicon has been playing an increasing role in the world of photonics because of the need for low cost and integrated optical transceivers in future computing systems. Such systems will rely ever more on multi-core architectures in which progress will be driven by interconnects as opposed to the switching speed of logic gates.

Because of the loss characteristics of optical fiber, data interconnects operate mostly in the 1550 nm region of the optical spectrum where fiber loss is at a minimum. Yet, at these wavelengths there is no direct absorption because the photon wavelength is insufficient to create free carriers (electron-hole pairs) across the energy bandgap. At high intensities however, silicon absorbs light via two photon absorption (TPA). While this effect is often problematic because it leads to a loss of light, it has been exploited to perform signal monitoring, data correlators and pulse compression at the 1550 nm wavelength band [1, 2, 3]. In this paper, we propose and validate via numerical simulations, a new device that exploits TPA and the floating body effect in a metal-insulator-silicon (MOS) transistor on SOI substrate. In our device, the floating body effect [4, 5] is exploited to create a large gain during conversion of 1550 nm wavelength photons to electrical current (or voltage). Conventional phototransistors are based on bipolar junction transistors that also offer large internal gain. Therefore, one can presumably use two photon absorption in these type of device to create long wavelength detectors. However, despite its high gain, a bipolar phototransistor suffers from large noise due to the low impedance of its input (base) terminal. On the other hand, an MOS device has very large input (gate) impedance resulting in much lower noise. Being an MOS structure, the proposed device is also completely compatible with standard CMOS process.

## 2 Floating body silicon phototransistor memory element

Figure 1 shows the basic structure of our proposed device. The n-p-n type MOS field effect transistor (FET) is placed at the end of the optical waveguide. As shown in Fig. 1 (b), once the light enters the FET body, the carriers are created by TPA. Owing to their higher velocity, electrons are swept out by the source-drain electric field resulting in a net population of holes in the channel. These holes modulate the gate voltage resulting in switching of the transistor output. This is the key concept in the photosensitivity of the proposed device which operates as a switching (digital) photodetector with hysteresis. In other words, the device functions as an opto-electronic memory.


DOI: 10.1587/elex.7.1790
Received November 07, 2010
Accepted November 16, 2010
Published December 25, 2010

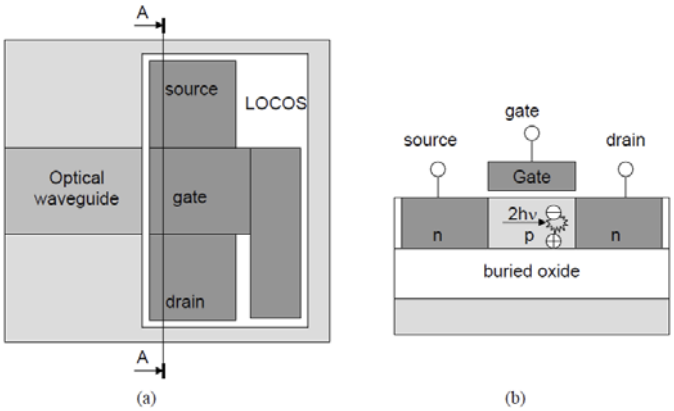



**Fig. 1.** Structure of Floating Body Silicon Phototransistor Memory. (a) Top view, and (b) Cross sectional view. In READ state, drain voltage is increased, whereas in RESET state, drain voltage is decreased in order to sweep the holes that remain in the body.

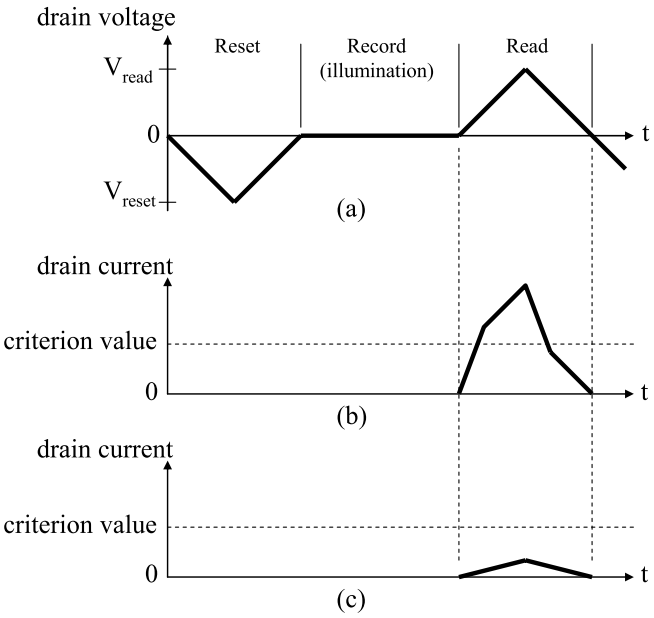



**Fig. 2.** Operation sequence of proposing device (a) and expected drain current profile at read state with recording (b) and without recording (c).

The operation sequence of proposing floating body silicon phototransistor memory element is shown in Fig. 2. The operation consists changing of drain voltage of the transistor and beam illumination on the body of the transistor. There are 3 states; Reset state, Record state, and Read state in operation sequence. At reset state, drain voltage is going down to minus to sweep out the remaining holes from the body of the transistor. At continuing record state, the drain voltage is kept to zero. The optical light through optical waveguide (shown in Fig. 1) is illuminated on the body to make recording. The carriers are created by TPA, and then a population of holes remain at body portion


DOI: 10.1587/elex.7.1790
Received November 07, 2010
Accepted November 16, 2010
Published December 25, 2010

after electrons swept out. At Read state, the drain voltage is going to plus and the drain current is to be monitored. Figure 2 (b), 2 (c) are profile of drain current when the light was illuminated or not illuminated during the record state, respectively. Because remaining holes at the body portion act as same with floating body effect, these holes reduce the threshold voltage of transistor. Therefore remaining holes can be detected by comparing the drain current value with criterion value. The drain voltage and gate voltage can be set to suitable value enough to have obvious dependence in drain current on light illumination.

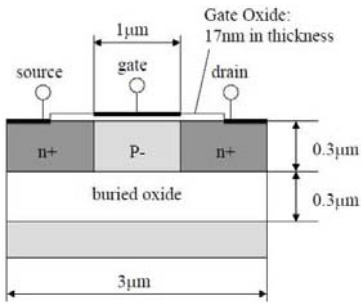
From the other point of view, by monitoring the drain current at read state, whether optical beam was illuminated or not illuminated during the recording state can be known.

## 3 Numerical validation

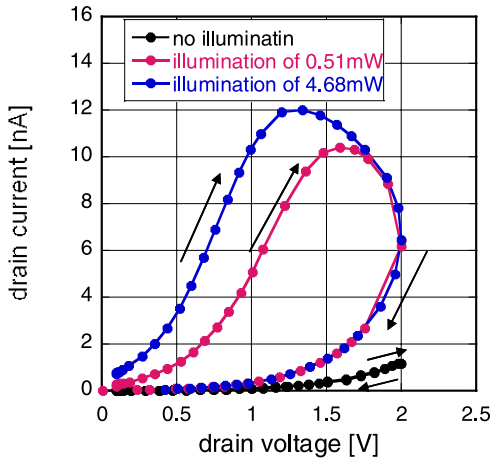
The device operation was validated using Altas device simulation tool from SILVACO Corporation which is one of the industry standard tools in CMOS device design and manufacturing. Device parameters used in the numerical simulation are shown in Fig. 3 (a). In idle mode, the MOS transistor is operated in the common source mode. The gate electrode is biased with a positive voltage (0.2 V) which is below threshold while drain voltage is set to 0 V (RECORD state). The simulation sequences is as following: first, the TPA induced carrier generation was included by the generation rate whose magnitude depends on the TPA coefficient of silicon $\beta$ and the optical intensity $I_p$, $\beta {I^2}_p/2E_p$, where $\beta = 0.7\,\mathrm{cm/GW}$, $E_p$ is the photon energy [6]. In this equation there is no time parameter, so we assume impulse light illumination, and TPA is instantaneous response such that free carrier absorption is avoided [7]. In our simulation, the body portion is uniformly illuminated. After illumination, free carriers recombination occurs and free carriers are also swept into drain or source portion. These are precisely calculated by the Device simulator, Atlas as in Ref. [6]. Thus, we obtain the distributions of remaining holes at the body portion. These steps are for memory writing. To read the devices, the drain voltage is increased to a positive value of 2 V (READ state) and the drain current is monitored. For the case of resetting, drain voltage is switched to a negative value of −2 V (RESET state).

The operation of this device as an opto-electronic memory is shown in Fig. 3 (b). In this figure, drain voltage is increased from 0 V to 2 V, followed by a decrease from 2 V to 0 V with the frequency of 1 kHz. MOSFETs with holes produced by TPA in the body have reduced threshold voltage and larger drain current. The large hysteresis suggests that floating body effects are probed. In Figure 3 (c), we show the dependence of the drain current on illumination power. Despite the low absorption of 1550 nm light in bulk silicon, the floating body effect, induced by the TPA generated carriers, is sufficient to switch the transistor with an optical power as low as 0.5 mW. In the simulation results, we use 1 cm as the unit length for gate width. It is known that the drain current is proportional to the gate width. So we need

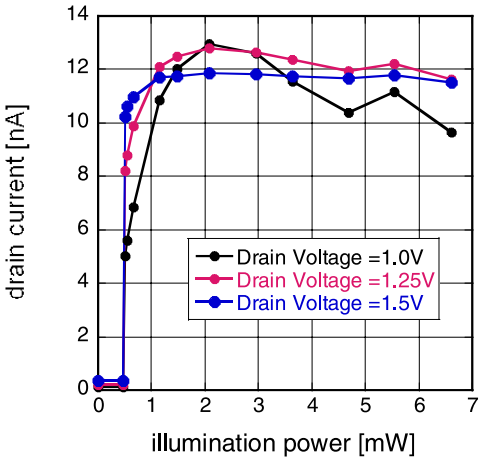

DOI: 10.1587/elex.7.1790
Received November 07, 2010
Accepted November 16, 2010
Published December 25, 2010




**(a).** Dimensions and conditions of the Silicon Phototransistor Memory used for numerical simulation. Doping concentration of n+ (source and drain) and p-(body) are 1.0e20 and 1.0e17, respectively. The gate width is 1cm.




**(b).** Dependence drain current on drain voltage for various illumination levels (Numerical simulation).




**(c).** Dependence of the drain current on the optical illumination power. (Numerical simulation). Drain current was monitored at 1.0V, 1.25V, and 1.5V in READ state.

**Fig. 3.** Device parameters of proposing device for numerical validation (a) and simulated results by Atlas device simulator (b) and (c).


DOI: 10.1587/elex.7.1790
Received November 07, 2010
Accepted November 16, 2010
Published December 25, 2010

to scale this calculated results with actual gate width. E.g. we have to divide the drain current by 1000 if the gate width is divided by 1000 (10 $\mu$m).

## 4 Discussion

We also evaluated the frequency response in read state. We remarked there is clear difference in drain current profile between with recording and without recording until the frequency of drain voltage is about 200 MHz. This is reasonable value for the gap length of 1 $\mu$m. To improve the frequency response of recording state, there are referential experimental results of modulation of Raman laser [7] and of electro-optical light modulator [8]. In both case, optical waveguides are located to intrinsic region of p-i-n structure to remove the carrier by applying the voltage to p and n electrodes. In the results, the transient times were about 200 ps which corresponds to 2 GHz operation. The distance between p-electrode and n-electrode is about 5 $\mu$m in Ref. [7, 8]. Further shrinking of the device dimensions can be done by reducing the waveguide dimension thus the gate length (body portion). Waveguide dimension can attain 0.08 $\mu$m size with small propagation loss introducing a taper structure [9]. It is known that reducing the gate length increase the operation frequency of the transistor. These can extend the frequency of transistor in both READ and RESET state, and reduce the transient time in RECORD state. So the miniaturization increases the operation frequency of our proposing device and enables us to attain the frequency of optical communication.

## 5 Conclusion

This validates the functionality of this device as a new switching (digital) photodetector that is completely compatible with standard CMOS device technology. This new device can be useful as a CMOS-compatible data buffer for on chip data communication between computing cores and between cores and conventional memory elements.

## Acknowledgments

Authors thank to Dr. Keunsam Rhee at SILVACO Japan Co., Ltd. for advising the programming of Atlas.


DOI: 10.1587/elex.7.1790
Received November 07, 2010
Accepted November 16, 2010
Published December 25, 2010