Fabrication of the semiconductor substrate for electric and photonic integrated circuits by pattern SIMOX method

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by

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Contents

Chapter 1 Introduction

1-1 Background

Based on an analysis published in June 2011 by International Data Corporation [1], a global electrical data created in 2011 reaches to 1.8 zeta byte which is nine times compared to the data in 2006. The expected global electrical data created in 2016 is eight times of 2011. So the growing rate of electrical data will be sustained. Individual contribution including downloading from web site is 75% of created electrical data. This growth of electrical data by individual indicates further accession of network traffic to the home which is located at the terminal of communication network.

According to a report from Japanese Ministry of Internal Affairs and Communications published in May 2011[2], the rate of internet usage at home reaches to 77.9% in 2010. The rate of optical communication path to home is 52.2%. This data shows optical communication path already reaches to the terminal of communication network and increasing of the electrical data created by individuals. In addition, increasing of optical communication path at the terminal indicates market growth of short distance optical communication.

On the other hand, in case of enterprise communication, in "TSUBAME 2.0" a supercomputer at Tokyo Institute of Technology launched in 2010, optical communication between rack mounts enables faster calculation. This shows a market of short distance optical communication is also important in enterprise business.

The market growth of short distance optical communication requires not only high functionality but also low cost to optical communication devices.

Electronic Photonic Integrated Circuits: EPIC is expected as a technology which solves both high functionality and low cost of optical communication devices. The reason of the expectation is based on the history of integrate circuits which brought high functionality and low cost. The EPIC implements both

electrical integrate circuits and optical circuits on a silicon substrate. EPIC can handle optical signals guided in an optical waveguide by adjacent electric devices, and can create optical signals from electric signals created on the same substrate. EPIC technology is based on the silicon photonics[4,5] which is optical waveguide circuits technology on silicon substrate, and CMOS (Complementary Metal Oxide Semiconductor) integrated circuits technology which is electric circuits technology on silicon substrate.

Comparing to CMOS integrated circuits technology which is mature technology with 15year precise technology roadmap by ITRS, silicon photonics is growing technology, so silicon photonics is needed to adjust to current CMOS integrated circuits technology in order to realize EPIC on silicon substrate.

This paper is related to a research of silicon waveguide technology which adjusts to CMOS integrated circuits technology.

In this chapter, silicon photonics technology will be reviewed, the purpose of this research is described, and a structure of this paper is shown.

1-2 Review of silicon photonics

Silicon photonics is a collective term of optical waveguide devices made on silicon substrate. And recently silicon photonics has many research activities. Silicon photonics uses two major characteristics of silicon material, the first characteristic is silicon is transparent for the light whose wavelength is longer than 1.1 μm, and the second characteristic is silicon dioxide is also transparent and has lower index than silicon. As a result, silicon photonics can attain well confined optical waveguide structure for 1.3μm and 1.5μm light utilized in optical communication systems brought by large relative index difference between silicon and silicon dioxide. The well confined optical waveguide structures can be manufactured at lower cost with using semiconductor facilities for VLSI.

The history of silicon photonics was started by R. A. Sorel and K.

Petermann [6-8] at the end of 1980s and the beginning of 1990s. At these years several material combinations were used, they are high-resistivity epitaxial silicon layer on highly doped silicon substrate (relative index difference $\Delta n=0.009$)[6], Ge-Si epitaxial layer on silicon substrate (relative index difference $\Delta n=0.1$)[8], and silicon bonded layer on silica substrate (relative index difference $\Delta n=2.05$)[8]. The most of research activities in these years were focused on optical waveguide characteristics. The representative of optical waveguide structure[6] in these years is shown in figure 1-1(a). The thickness of Si-Ge layer is 7μm and rib height and width are 2.8μm and 10μm respectively.

At the latter 1990s, research activities using SOI (Silicon-on-Insulator) substrate which has buried oxide (BOX) layer were started[9-11], and researches on passive functional optical waveguide devices were appeared, for example, they are optical star coupler [12] and phased-array wavelength multi-demultiplexer [13]. But SOI substrates in these researches[9-13] are BE-SOI (bond and etchback silicon-on-insulator) substrates, so surface silicon layer has 5-11μm thick. The single mode optical waveguide condition can be realized only with rib waveguide structure having silicon dioxide clad layer. In addition the minimum width of optical waveguide is 2 or 3μm, so propagating optical light is not well confined. The representative of optical waveguide structure[9] in these years is shown in figure 1-1(b).

Between latter 1990s and 2000, SmartCut [14] and SIMOX[15] were developed which are fabricating technologies of BOX substrates for VLSI. As SOI substrate fabricated by SmartCut or SIMOX with thin silicon layer in the range from 0.1μm to 1μm and with high quality began to supply, characteristics of electrical circuits and optical waveguide devices were rapidly upgraded. In the field of electrical circuits with SOI substrate, PowerPC processor is manufactured by IBM from 2000[16]. In 2005 when the game machine: Playstation3 using Cell Processor developed by 3 company-collaboration (IBM, Toshiba, and Sony) was launched, the mass-production technology of CMOS LSI circuit on 300mm SOI substrate had been completed. In the field of optical waveguide devices with SOI

substrate, strip-type waveguide called “silicon wire” realized well confined optical waveguide brought by large relative index difference between silicon and silicon dioxide appeared, and passive type optical filter device with microring resonator made of very small cross-section of 0.4μm x 0.2μm and 2.5μm radius waveguide were reported[18]. The single mode conditions of strip type optical waveguide were reported that the crosssection of waveguide is less than 0.3μm x 0.3μm[19] or 0.32μm x 0.5μm[20]. Therefore the optical waveguide of cross-section of 0.4μm x 0.2μm is single mode condition.

On the other hand, research activities on optical waveguide with nonlinear effect like Raman laser [21, 22] appeared with using precise fabrication technology and high quality silicon layer.

In the aspect of a function of optical waveguide device, researches in optical modulator went ahead compared to researches in emitting device and detector. Lipson reported optical light modulator with pn structure in microring resonator[23]. In 2005, Intel reported Mach-Zehnder type optical light modulator operated at 10GHz[24]. Reed demonstrated 50GHz operation in Carrier-depletion type optical modulator[25]. And Enablence reported optical communication device with Mach-Zehnder interferometer[26].

The optical waveguide structure is not only strip type[18, 23] shown in figure 1-1(c), but also ridge type[21, 22, 24, 26] shown in figure 1-1(d). The different waveguide structure is used for each application.

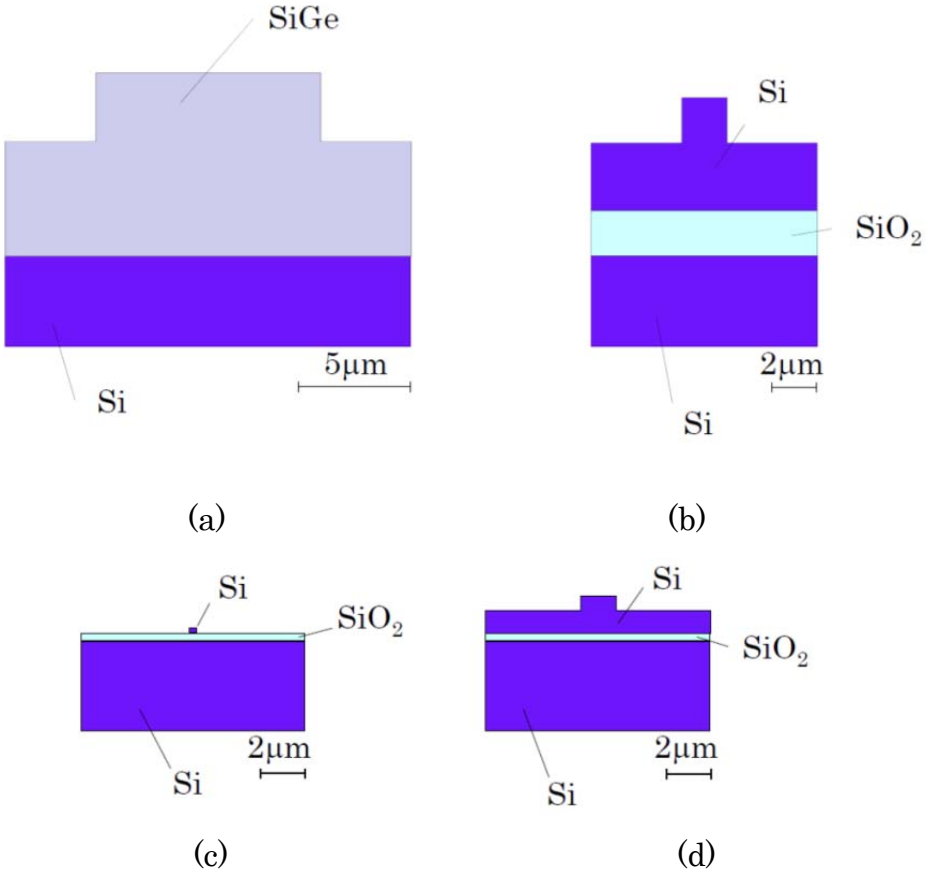


Figure 1-1 Transition of optical waveguide in silicon photonics.
(a) R. Soref and J. Lorenzo in 1986[6], (b)P. D. Trinh, etal in 1995 [9]
(c) K. Yamada, etal in 2003 [18], (d) L. Liao, etal in 2005 [24]

Regarding light detector, with research activities on forming Ge layer on silicon substrate in latter 2000s[27, 28], the characteristics of Ge light detector has great improvement in frequency response and sensitivity in this 5 years[29, 30]. Kotura reported Ge detector with 1.1A/W sensitivity and 32GHz (-3dB) frequency response at 1.55μm wavelength in 2009[31], so Ge type light detector is close to practical use.

On the other hand regarding light emitting devices, research activities using Ge material are also rapidly progressing. Kimerling reported direct-gap photoluminescence[32] and electroluminesence[33] using Ge material in 2009, and photoexcited type 1.59-1.61μm laser in 2010. So current injected type laser is

thought to be reported soon. There is another research activity using hybrid structure made of silicon and group III-V compound material that is already commercialized as independent laser devices with higher emitting efficiency.

Bowers of University California, Santa Barbara applied bonding technology of group III-V compound laser on silicon substrate and introduced the light from the laser into optical waveguide in silicon layer[35], and demonstrated the wavelength-variable laser tuned by Bragg reflector in 2008[36].

In 2006, the combination with CMOS integrated electrical circuits and optical waveguide on SOI substrate was reported by Luxtera as optical communicating device[37]. This result was the first demonstration of EPIC. The demonstration of 40GHz optical transceiver was also reported by Luxtera with the combination of 130nm rule CMOS circuits and optical waveguides[38]. This optical transceiver device had no laser devices but had 40GHz optical modulators and optical detectors.

In latter 2000s two decade old from Soref's papar in 1986, silicon photonics had many type of candidate devices. At present, preparing of combination of CMOS circuits is going.

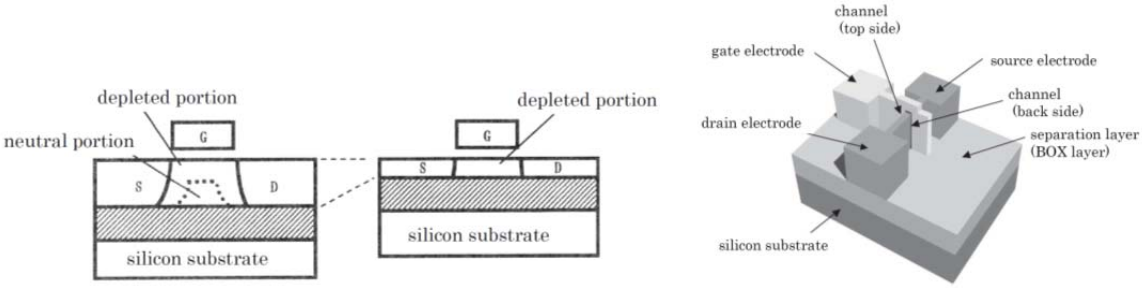
1-3 Structures of SOI transistors and directional movement of SOI substrate

Because transistors fabricated on SOI substrate are electrically isolated by BOX layer from substrate, performance of the transistor is faster than transistors on bulk silicon substrate owing to small floating capacitance. In addition, power consumption of the transistor on SOI is smaller owing to small leak current to substrate[16].

There are two types of transistor on SOI substrate, one is partially depleted-SOI (PD-SOI) and another is fully depleted-SOI (FD-SOI)[15]. The difference between two types is in depleted region. In FD-SOI transistor, the all area of body portion from just beneath gate oxide to boundary of BOX layer is

depleted at operation. In PD-SOI transistor, partial area of body near gate oxide portion is depleted at operation. Reference 15 defines that PD-SOI transistors are made on the SOI whose top silicon layer has 80-200nm thick, and FD-SOI transistors are made on the SOI whose top silicon layer has 60-80nm thick.

Recently, Fin-FET transistor whose operating speed is faster than FD-SOI or PD-SOI was reported[39]. Figure 1-2 shows the structures of transistor on SOI[39, 40]. In Fin-FET, BOX layer acts as separation layer and the direction of electric field is parallel to in-plane direction of SOI substrate. As shown in figure 1-2, there is a huge difference in structure between transistor types.



(a) PD-SOI (b) FD-SOI (c) Fin FET

Figure 1-2 Comparison of transistors on SOI[39, 40].

There is no need to say, bulk silicon substrate is common for all type of transistors fabricated on bulk silicon substrate despite the progress of design rule. But in the technology of PD-SOI and FD-SOI, thinner surface silicon layer is required as the progress of design rule[41, 42]. Luxtera used SOI substrate whose surface silicon layer is 220nm thick, and the thickness of 220nm is suitable thickness of 130nm design node of PD-SOI by Freescale Semiconductor, Inc. So thinner thickness of surface silicon layer is required when shorter gate length is applied. In FD-SOI, the thickness of surface silicon layer is required to be less than 10nm when the gate length is shorter than 30nm[42]. In Fin-FET 15nm is the suitable thickness of surface silicon layer in currently developed Fin-FET whose gate length is 20nm.

From the aspect of the characteristics of transistor fabricated on SOI,

directional movement of SOI is thinner thickness of surface silicon layer.

1-4 Purpose of research

EPIC on silicon substrate is regarded as the best device for coding and decoding signal processing including advanced scrambling with a secret code at low cost because the signal processing is performed at the closest portion to optical waveguide on the same silicon substrate. Figure 1-3 shows the photograph of Luxtera's EPIC device[37]. Figure 1-4 shows the conceptual diagram of the devices. As shown in figures 1-3 and 1-4, silicon layer of electrical circuits and silicon layer of optical waveguide are same. The silicon layer is required to be divided into electrical circuit area and optical waveguide area with enough buffer area. By adding optical waveguide, the area of electrical circuits is reduced by area of optical waveguide and the buffer area.

As mentioned above, surface silicon layer of 220nm thick is suitable for the thickness of CMOS circuits with 130nm node PD-SOI and single mode condition of well confined silicon wire optical waveguide with 400-500nm width. The additional process such as epitaxial growing on optical waveguide area might be required in order to obtain well confined condition when thinner surface silicon layer is applied suitable for narrower design rule in CMOS circuits.

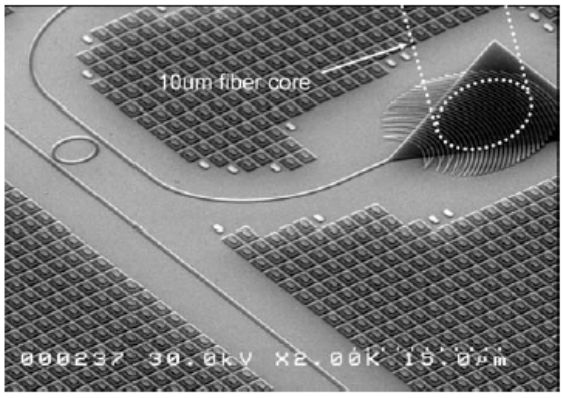


Figure 1-3 Photographs of Luxtera's EPIC[37].

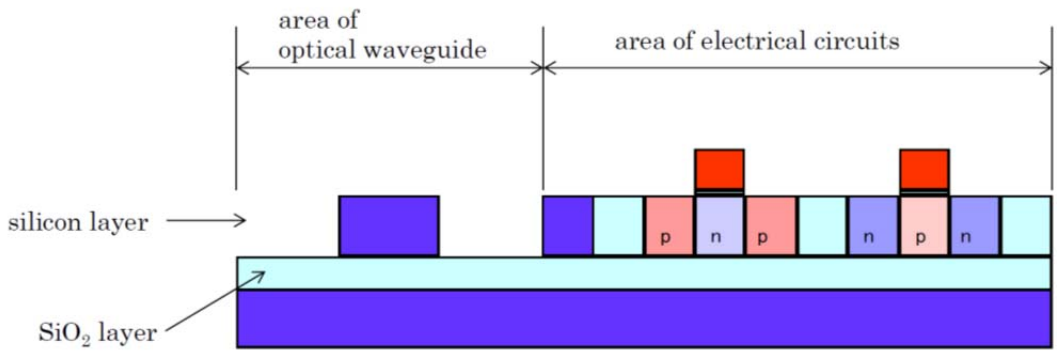


Figure 1-4 Conceptual diagram of Luxtera's EPIC.
Electrical circuits and optical waveguide are fabricated on same silicon layer

The author proposed the EPIC structure that optical waveguide is fabricated on the second silicon layer from the surface and reduction of electric circuit area is to be minimum by the separation of layers of electrical circuits and optical waveguide. The proposed EPIC structure is shown in figure 1-5. In the proposed EPIC structure, there is no need to coincide thickness of silicon layer of electrical circuits and thickness of silicon layer of optical waveguide. It has the characteristic of availability that thickness of silicon layers can be suited for electrical circuits and optical waveguide independently.

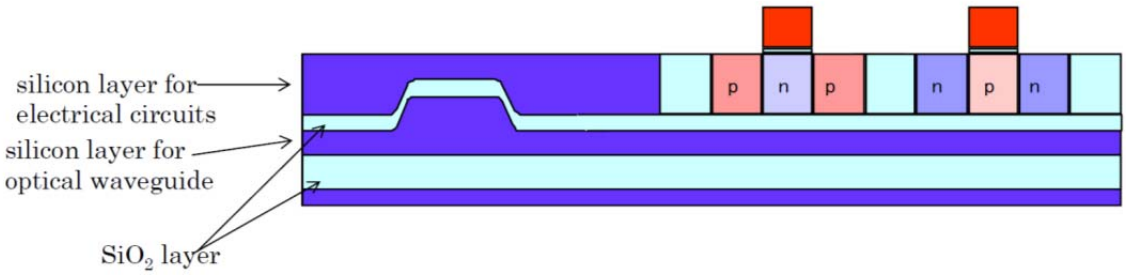


Figure 1-5 Conceptual diagram of proposed EPIC.
Electrical circuits and optical waveguide are fabricated in different silicon layer

The main purpose of this research is to establish fabricating technology of optical waveguide on the second layer from the surface by pattern SIMOX as a

compatible technology with CMOS electrical circuit technology. And technology of the pointing depth of defect suitable for total inspection is proposed and demonstrated as a required technology in fabrication of electrical circuits on the surface silicon layer. In addition as required in design process of integrated circuits of electrical circuits and optical waveguide circuits, the interaction of electrical device and optical device is scientifically clarified in order to establish the electrical and photonic integrated circuits on SOI substrate technology made by pattern SIMOX.

1-5 Framework of thesis

Framework of this thesis is shown in figure 1-6.

In chapter 1, requirement of optical communication device is not only high functionality but also low cost because of business expansion of short distance optical communication as a background of this research, and EPIC is expected as the technology which solves both requirements of optical communication devices. The main purpose of this research is described to establish fabricating technology of optical waveguide on the second layer from the surface by pattern SIMOX as a compatible technology with CMOS electrical circuit technology.

In chapter 2, SIMOX technology that is a fabrication technology of current CMOS grade SOI substrate is summarized, and results of fundamental examination are shown. The reason of application of pattern SIMOX in this research is described and positioning of this research is clearly shown with the analysis of the previous research on pattern SIMOX. From examination of SIMOX process to SOI substrate, characteristic of SOI substrate with double BOX layer made by SIMOX that there are defects in second silicon layer from the surface despite no defects in surface silicon layer is shown.

In chapter 3, research of non-destructive and effective defect pinpointing technology that can distinguish the defect position among surface silicon layer for

electrical circuits, second silicon layer for optical circuits, and bulk silicon layer is described. Although the amount of 9TB in data size is created by existing optical defect inspection with fluorescent microscope is implemented on a 300mm silicon substrate, the proposed method can reduce the data size to from 1/10 to 1/20 despite 100nm depth resolution.

In chapter 4, research of pattern SIMOX technology to fabricate optical waveguide in second silicon layer in keeping with enough quality of surface silicon layer for CMOS electrical circuits is described. The process flow of SIMOX buried optical waveguide compatible with CMOS electrical circuits on surface layer is obtained. Through this research, phenomena that defects are created when buried oxide layer is separated and buried oxide profile coincide to ion implantation profile is successfully created by blocking the oxide in annealing process from the ambient are obtained.

In chapter 5, research on the device using interaction between vertically stacked SOI transistor and optical waveguide is described. The SOI transistor memory device with two-photon absorption by illumination of 1.55μm light on body portion, residual hole at body portion, and floating body effect is proposed and validated.

In chapter 6, the thesis is concluded. The available configuration of electrical and photonic integrated circuits is disclosed and applications of obtained technologies through this research are described.

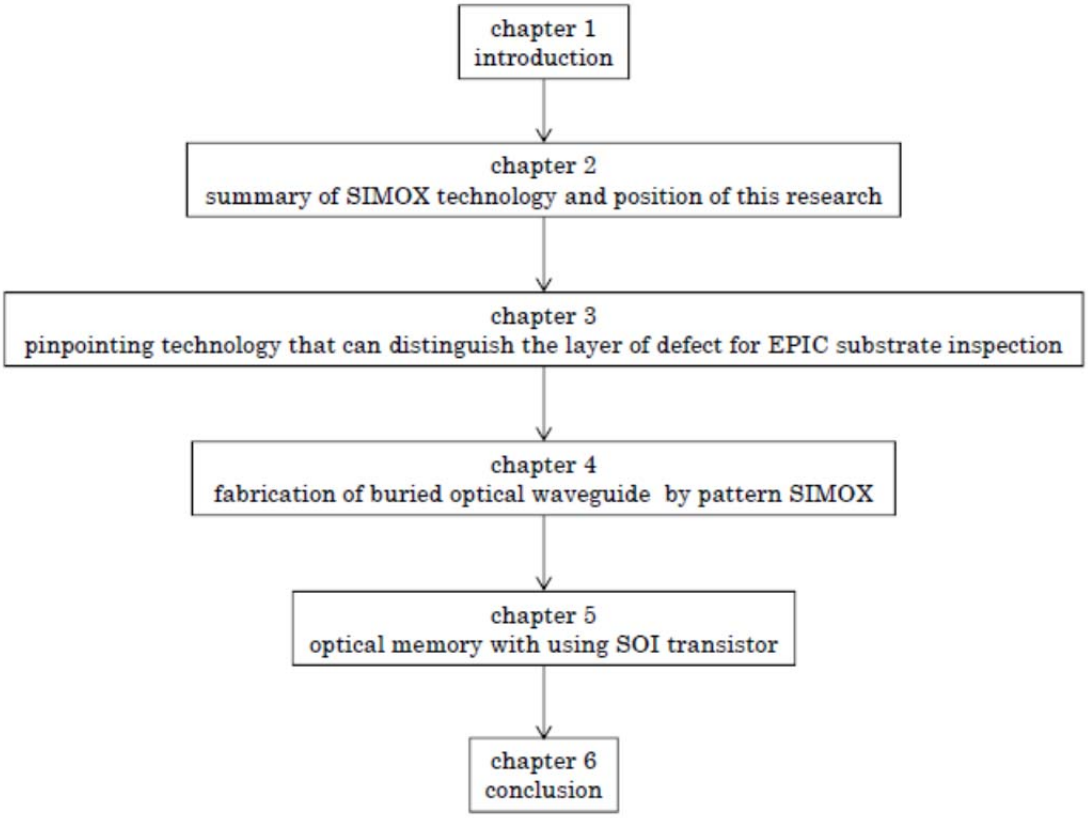


Figure 1-6 Framework of this thesis.

Chapter 2 Summary of SIMOX technology and position of this research

2-1 Introduction

In this chapter, two manufacturing methods of SOI substrate for CMOS electrical circuits are summarized in order to accomplish the research purpose of this research "to establish fabricating technology of optical waveguide on the second layer from the surface by pattern SIMOX as a compatible technology with CMOS electrical circuit technology". The reason of application of pattern SIMOX in this research is described. The pattern SIMOX technology to fabricate optical waveguide in second silicon layer in keeping with enough quality of surface silicon layer for CMOS electrical circuits is proposed through the analysis of the previous research on SIMOX and pattern SIMOX. From examination of SIMOX process to SOI substrate, characteristic of SOI substrate with double BOX layer made by SIMOX is studied. The obtained result is that there are defects in second silicon layer from the surface despite no defects in surface silicon layer. Small defects are negligible for optical circuits but are not negligible for electrical circuits because of device size. Because the distance between silicon layers of electrical circuits and optical circuits is less than 1μm, the requirement of non-destructive and effective defect pinpointing technology that can distinguish the defect position between two silicon layers is clarified. The positioning of this research is clearly shown by defining challenges in this research.

2-2 Fabrication methods of CMOS grade SOI substrate

To fabricate optical waveguide underneath the surface, patterning of silicon dioxide is required. The patterning method of silicon dioxide is required to be CMOS compatible because CMOS transistors are fabricated at the surface silicon layer. As of 2011, there are only two fabrication methods that creates

buried silicon dioxide layer, they are SmartCut method[14] and SIMOX method[15]. In this section, two fabrication methods are summarized and discussed regarding to the application in this research.

2-2-1 SmartCut method

Process of SmartCut is shown in figure 2-1. This method uses two silicon bulk substrates A and B. (a) Hydrogen ion implantation is performed to one bulk silicon substrate A. And subsequently thermal oxidation on two substrates A and B is performed for wafer bonding. (b) Wafer bonding process is performed. (c) Wafer separation process that includes precipitation of implanted hydrogen and creation of SiH_4. Because SiH_4 is gas state, substrate separation is caused at the depth of hydrogen implantation. (d) Touch polishing is performed to obtain enough smooth surface for CMOS electrical circuits. In addition, substrate A can be reused.

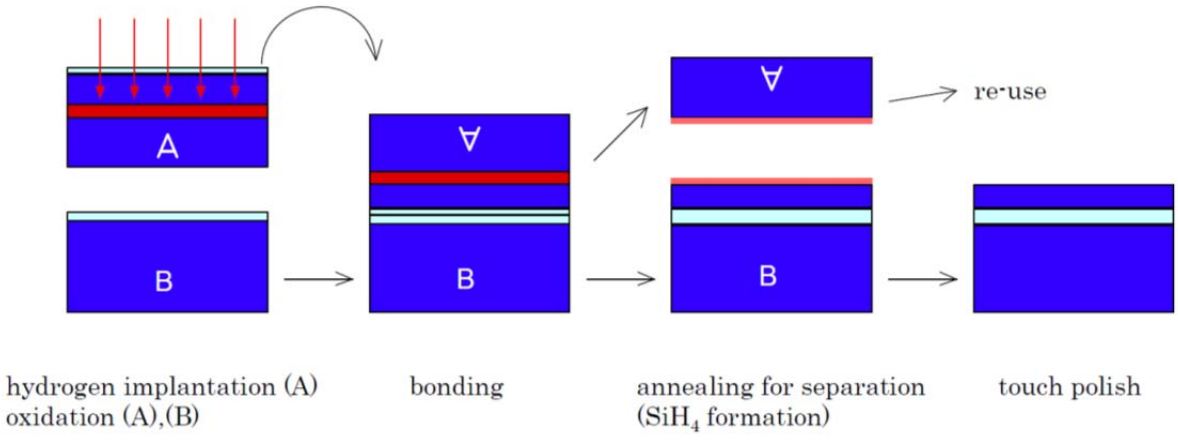
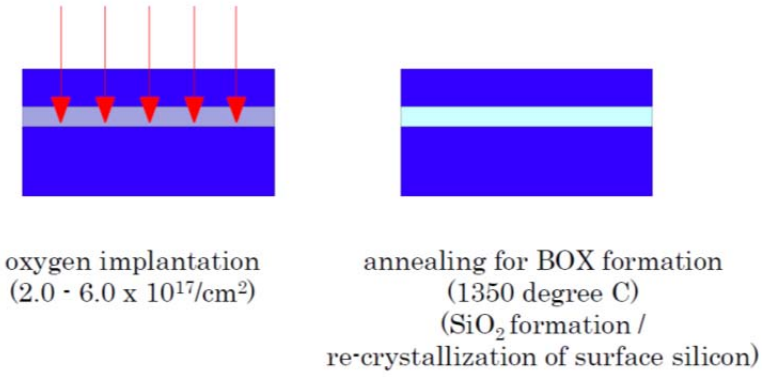


Figure 2-1 Fabrication method of SOI for CMOS grade 1; SmartCut [14].

2-2-2 SIMOX method

The process of SIMOX is shown in figure 2-2. SIMOX SOI substrate is composed of one silicon bulk substrate. (a) Oxygen Ion implantation is performed. Dose of oxygen is much larger than dose of hydrogen in SmartCut process. And oxygen has larger atomic weight than hydrogen. Crystalline properties are almost lost at the passing area of oxygen ion after ion implantation. (b) The high temperature annealing between 1300 and 1350 degree C creates SiO_2 layer near ion implantation area and recovers crystalline properties of silicon by re-crystallization.



(a) (b)

Figure 2-2 Fabrication method of SOI for CMOS grade 2; SIMOX method[15].

2-2-3 Selection of fabrication method for buried optical waveguide formation

From the aspect of optical waveguide beneath surface of silicon substrate, two methods are compared. In case optical waveguide is composed of two pure material; silicon and silicon-dioxide, the sub-micron range thickness modulation of silicon layer is required in order to make rib waveguide or strip waveguide. Because SmartCut requires flat surface at the bonding process, buried oxide layer must be flat. The thickness modulation portion should be made at the surface.

Consequently, the flat surface cannot be obtained if we select SmartCut method. For this reason, SIMOX method is selected for buried optical waveguide formation beneath the surface, and the fabrication of SOI substrate which can integrate both electrical devices and optical devices is investigated in this research.

2-3 Review of SIMOX method for SOI substrate

The acronym of SIMOX (Separation by implanted oxygen) was named by Izumi of NTT. In Izumi's paper[43] published in 1978, oxygen ion implantation to bulk silicon substrate was performed at 150keV and following high temperature annealing at 1150 degree C creates SOI substrate with buried SiO_2 layer (BOX: Buried Oxide), and operation of ring oscillator circuit using CMOS transistors was demonstrated. Results on SIMOX before 1980s including Izumi's work were summarized by P.L.F. Hemment of University of Surrey in 1986[44]. Dose value of ion implantation in these results are $1.0 - 2.0 \times 10^{18}/cm^2$, are twofold of current dose.

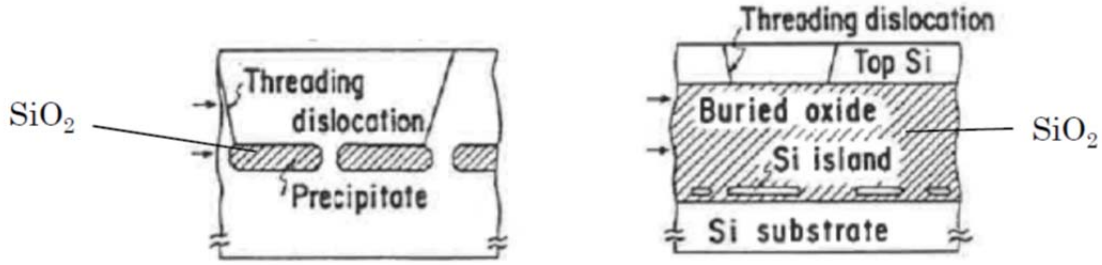
Through extensive researches on acceleration voltage of ion implantation[45, 46], on dose value[47], and out-diffusion and in-diffusion of oxygen in annealing process[48], several optimized SIMOX conditions supposed for sophisticated CMOS circuits were obtained from 1990s to 2000. P.L.F. Hemment of University of Surrey reported the conditions of dose of $3.3 \times 10^{17}/cm^2$ at acceleration voltage of 70keV[49]. Meng Chen of Chinese Academy of Science reported the conditions of dose of $4.5 - 5.5 \times 10^{17}/cm^2$ at acceleration voltage of 160keV[50] and reported that there was optimum condition in the range of dose of $2.5 - 5.5 \times 10^{17}/cm^2$ by adjusting accelerated voltage[51]. Ogura of NEC reported high-quality SOI substrate with low defects density could be obtained at dose of $2.0 - 6.0 \times 10^{17}/cm^2$ at acceleration voltage of 180keV by applying the optimized annealing process[52]. Ibis Technology Corporation who is the manufacture of specialized ion implantation machine for SIMOX and Mitsubishi Material

Corporation jointly reported the conditions of dose of 4.0 x $10^{17}/cm^2$ at acceleration voltage of 175keV[53] and conditions of dose of 2.0 – 2.5 x $10^{17}/cm^2$ at acceleration voltage of 65keV[54, 55]. They launched the mass production of SOI substrate for CMOS integrated circuits. SIMOX methods for high quality SOI substrate with low defects density at dose of 2.0 – 6.0 x $10^{17}/cm^2$ are categorized into low-dose SIMOX method, and SIMOX methods at dose of 1.0 – 2.0 x $10^{18}/cm^2$ summarized by P.L.F. Hemment [44] categorized into high-dose SIMOX method[15].

Izumi of NTT reported a method to increase the thickness of buried oxide (BOX) layer by annealing at high concentration of oxygen, named ITOX (internal thermal oxidation), and reported the condition of dose of 4.0 x $10^{17}/cm^2$ at acceleration voltage of 180keV + ITOX[56]. Matsumura of Siltronic Japan reported that ITOX method was able to widen the dose condition to 3.0 – 4.0 x $10^{17}/cm^2$ at acceleration voltage of 180keV[57]. And Siltronic Japan started the mass production of SOI substrate for CMOS integrated circuits.

In the mass production of SOI substrate by SIMOX method, ITOX method is effective because ITOX reduces the operation time of ion implantation machine which is the most expensive among mass production machines of SIMOX method.

Figure 2-3 shows the defect types of buried oxide (BOX) layer of SOI substrate fabricated by SIMOX method. Figure 2-3(a) shows the discontinuity of BOX layer caused when insufficiency of dose at ion implantation or existence of particles on the surface at ion implantation. Figure 2-3(b) shows residual silicon portion in BOX layer called silicon island caused when excess of dose at ion implantation. Both defect types might bring degradation of insulating performance of BOX layer.



(a) (b)

Figure 2-3 Defect types of buried oxide (BOX) layer by SIMOX method[47]

By summarizing the above reviews of SIMOX method, several optimized SIMOX conditions exist for SOI substrate with uniform BOX layer by applying uniform ion implantation. In the range of dose of 2.0 – 6.0 x $10^{17}/cm^2$, optimized SIMOX conditions of SOI substrate for sophisticated CMOS circuits are expected by adjusting accelerated voltages and annealing process.

2-4 Review of pattern SIMOX method

In this section, previous researches of SIMOX method with partial ion implantation of oxygen called pattern SIMOX method or local SIMOX are summarized.

The purpose of obtaining local SOI substrate by pattern SIMOX method is integration of arithmetic circuits with CMOS on SOI and DRAM which is cheap data memories on bulk silicon substrate. The most popular and cheapest DRAM used in semiconductor field is capacitor type memories. The capacitor type memories apply the structure of fine and deep hole with oxide film and electrode on side wall of the hole on bulk silicon substrate for larger capacitance at small foot print to have higher performance of long-term recording and recording density. It is impossible to apply high-density capacitor type DRAM memories on SOI substrate because of existence of insulating BOX layer. From this reason, as shown in figure 2-4, the integration of arithmetic circuits with CMOS on SOI and

DRAM by applying pattern SIMOX was attempted. The beginning of the attempt was reported by P.L.F. Hemment of University of Surrey in early 1990s[58, 59] before mass production of SOI substrate for CMOS integrated circuits. Fraunhofer Institute[60] and IBM[61] reported attempt of pattern SOI in about 2000. Despite these attempts, cracks at the boundary of ion implantation area were unavoidable because the volume increases of 2.27 times when silicon changes to silicon dioxide as shown in figure 2-5. Figure 2-6 shows the crack at the boundary of ion implantation reported by IBM[61].

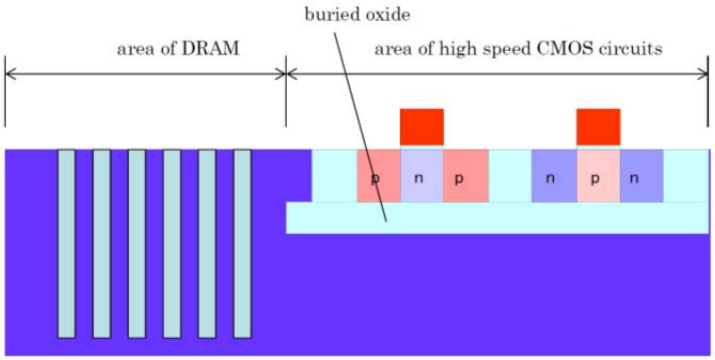


Figure 2-4 Pattern SOI substrate attempted by pattern SIMOX[58-61]

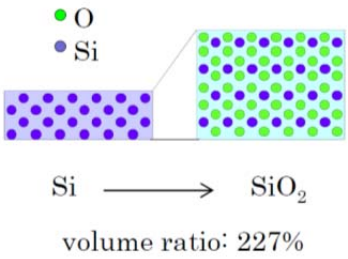


Figure 2-5 Volume expansion when silicon changes to silicon dioxide

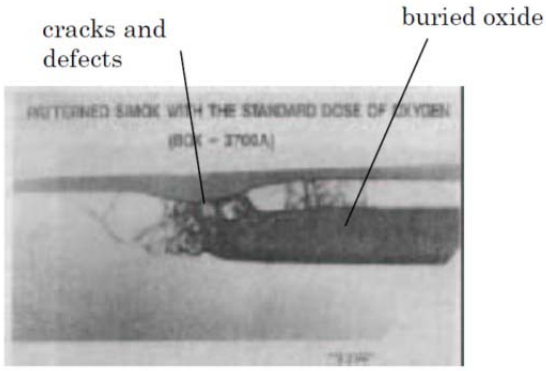


Figure 2-6 Experimental result of pattern SIMOX by IBM[61]

Mang Chen of Chinese Academy of Science reported two SIMOX conditions of dose of 2.0 x $10^{17}/cm^2$ at acceleration voltage of 50keV[62] and dose of 3.5 x $10^{17}/cm^2$ at acceleration voltage of 100keV[63] which avoid crack at the boundary of ion implantation. Figure 2-7 shows the experimental results by SIMOX condition of dose of 3.5 x $10^{17}/cm^2$ at acceleration voltage of 100keV[63]. From this picture the BOX layer is not symmetric, so created BOX layer does not reflect profile of ion implantation correctly.

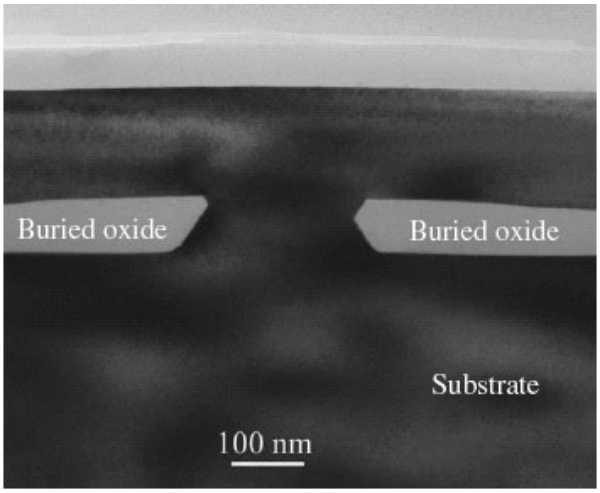


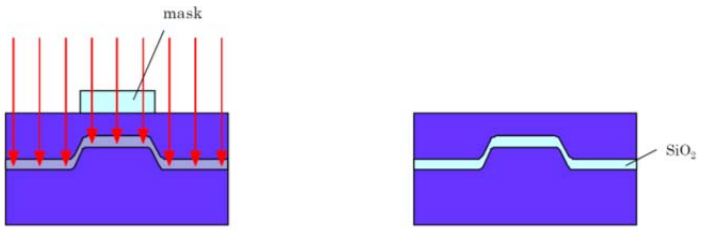
Figure 2-7 Experimental result of pattern SIMOX by Meng Chen [63]

By summarizing the above reviews of pattern SIMOX method, partial and non-uniform ion implantation produces crack or uncontrollable BOX shape at the

boundary of ion implantation area. It is supposed to be very difficult to fabricate low defects SOI substrate for partial and non-uniform ion implantation SIMOX method.

2-5 Optical waveguide fabrication by pattern SIMOX with transparent mask

From the reviews of previous research of pattern SIMOX, partial and non-uniform dose ion implantation cannot create BOX layer reflected ion implantation profile correctly without defects[60-63]. In this thesis, optical waveguide fabrication by pattern SIMOX with transparent mask is proposed. This proposal is derived from the reason that uniform dose ion implantation at modulated depth reduces the stress by volume expansion of silicon to silicon dioxide and correct reflection of ion implantation fabricates optical waveguide underneath the surface by applying the transparent mask in ion implantation. Simplified process flow of the proposed method is shown in figure 2-8. Figure 2-8(a) oxygen ion implantation is performed through transparent patterned mask. Figure 2-8(b) high temperature annealing creates BOX layer with depth modulation.

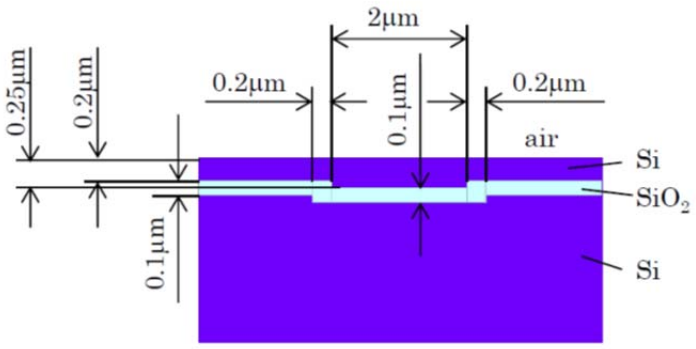


(a) (b)

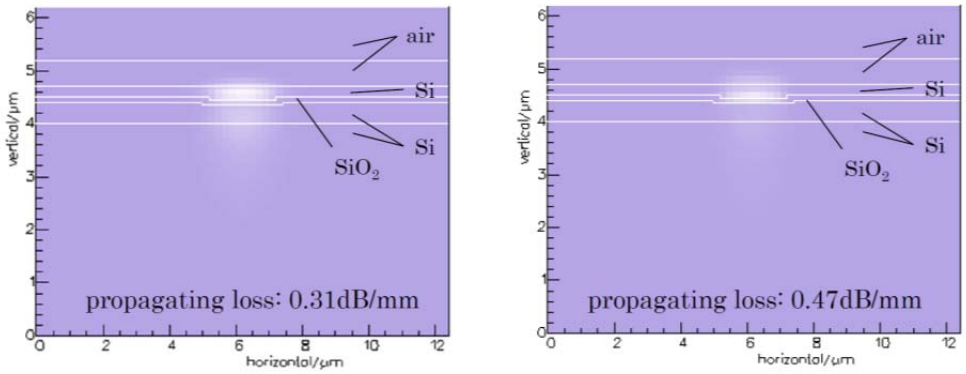
Figure 2-8 Proposed pattern SIMOX method with transparent mask

Properties of optical waveguide fabricated by pattern SIMOX method with transparent mask are discussed. Figure 2-9 shows the calculated properties of guiding mode and its propagating loss on the rib type optical waveguide fabricated on the surface. FIMMWAVE; a commercialized solver of beam

propagation method from Photon Design (http://www.photond.com/) was used in calculation. Because BOX thickness of SOI substrate fabricated by low-dose SIMOX is about 100nm, thickness of buried oxide is set to 100nm as shown in Figure. 2-9(a). Figures 2-9(b) and (c) show electric field distribution and propagating loss of optical waveguide in TE mode and TM mode, respectively. From this result there are large propagating loss of 0.31dB/μm (TE mode) and 0.47dB/μm (TM mode) at 1.55μm wavelength light because of the weak confinement in the substrate direction.



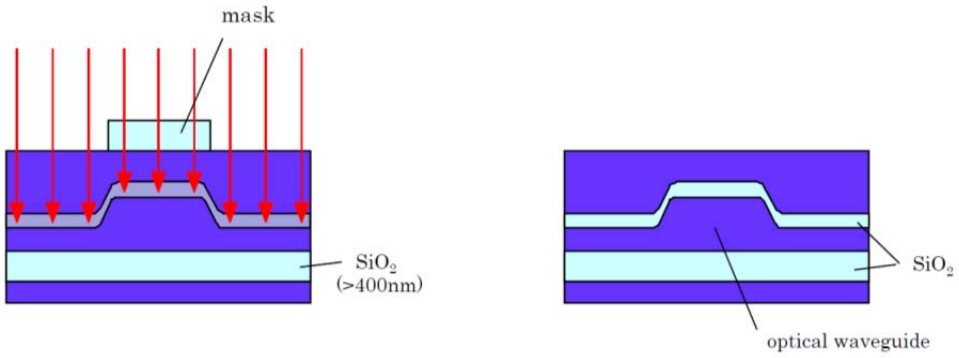
(a)



(b) (c)

Figure 2-9 Propagating mode and loss of optical waveguide by pattern SMOX. (wavelength: 1.55μm)
(a) Structure of optical waveguide in simulation
(b) Electric field distribution of propagating light in TE mode
(c) Electric field distribution of propagating light in TM mode

Rickman reported that the minimum thickness of buried oxide is 0.4μm to have enough confinement with suppression of substrate radiation of propagating light in silicon optical waveguide.[64] Therefore optical waveguide fabrication method composed of pattern SIMOX process onto an SOI substrate with more than 0.4μm thick BOX layer applying the transparent mask in ion implantation is proposed. The simplified process flow is shown in figure 2-10. Figure 2-10(a) oxygen ion implantation is performed onto SOI substrate with 0.4μm thick BOX layer through transparent patterned mask. Figure 2-10(b) high temperature annealing creates BOX layer with depth modulation.



(a) (b)

Figure 2-10 Optical waveguide fabrication method composed of pattern SIMOX applying the transparent mask

2-6 Features of vertically stacked EPIC

In this section features of EPIC circuits in which CMOS electrical circuits and optical circuits were vertically stacked in thickness direction are described.

Feature 1: Reduction of restrict conditions in layout design

Vertical placement of CMOS electrical circuits and optical circuits expands CMOS electrical circuit area comparing to lateral placement. In case CMOS electrical circuits and optical circuits are placed on the same silicon layer, it is

difficult to across the optical circuit area for electrical circuits and to allocate optical waveguide in electrical circuit area. By allocating different silicon layers for CMOS electrical circuits and optical circuits, restrictions in layout designing are dramatically reduced.

Feature 2: Independent setting of silicon thickness

The suitable silicon thickness for CMOS electrical circuits is getting thinner according to the evolution of CMOS design rule. When CMOS electrical circuits and optical circuits are allocated to different silicon layers, silicon thickness for CMOS electrical circuits can be set to suitable thickness regardless of optical circuit conditions. On the other hand, the silicon thickness of optical circuits can be set to thicker than 220nm which is the thickness of Luxtera's EPIC, so ridge type optical waveguide can be employable.

Feature 3: Availability of vertically stacked optical circuits

By allocating a part of silicon layer of CMOS electrical circuit area to optical circuits, vertically stacked optical circuits are attainable. Optical coupling between vertically stacked optical waveguides is achieved and multiply aligned vertically coupled micro-ring resonators as shown in figure 2-11 are easily provided.

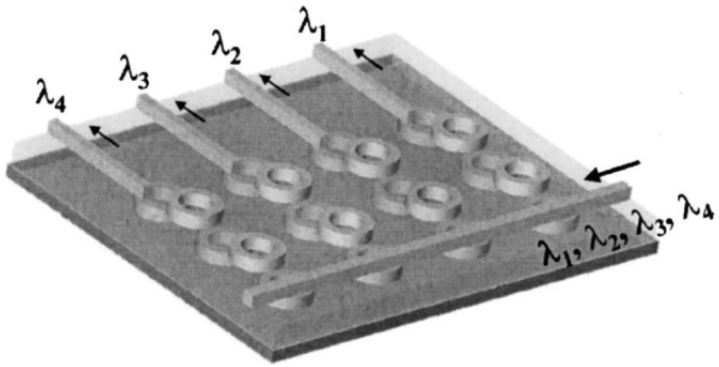


Figure 2-11 Multiply aligned vertically coupled micro-ring resonators

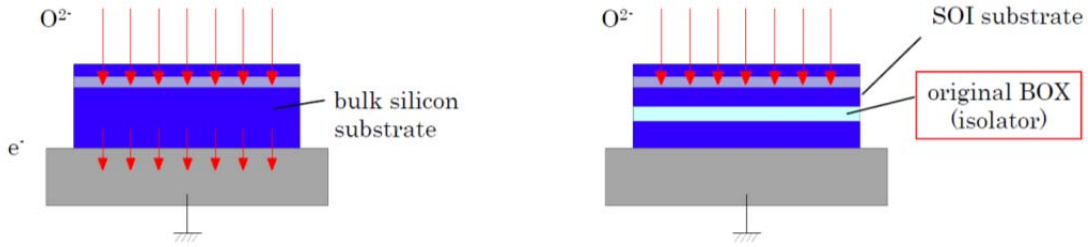
2-7 Experiment of uniform SIMOX on flat SOI substrate

2-7-1 Purpose of the experiment

There are some differences between waveguide fabrication into the second silicon layer from surface using SIMOX process on SOI substrate and normal SIMOX process which makes SOI substrate. The differences are written in the followings.

1. The substrate on which SIMOX process is applied is SOI.
2. There are mask patterns on the substrate in SIMOX.

As shown in figure 2-12, when the substrate on which SIMOX process is applied is SOI, implanted charges might be stayed and cause damage by the presence of BOX layer. So this experiment is required. The purpose of this section is to examine the quality of surface silicon layer and uniformity of buried oxide layer when normal SIMOX process which makes SOI substrate for CMOS electrical circuits is applied to SOI substrate.



(a) (b)

Figure 2-12 Comparison of SIMOX process in ion implantation
(a) normal SIMOX process which makes SOI substrate
(b) fabrication of optical waveguide in second silicon layer from the surface

2-7-2 Method of uniform SIMOX on flat SOI substrate

The SIMOX condition of dose of 4.0 x $10^{17}/cm^2$, acceleration voltage of 180keV and ITOX [57] is applied in this experiment. Siltronic Japan corporation uses this SIMOX condition in mass production of SOI substrates for CMOS electrical circuits.

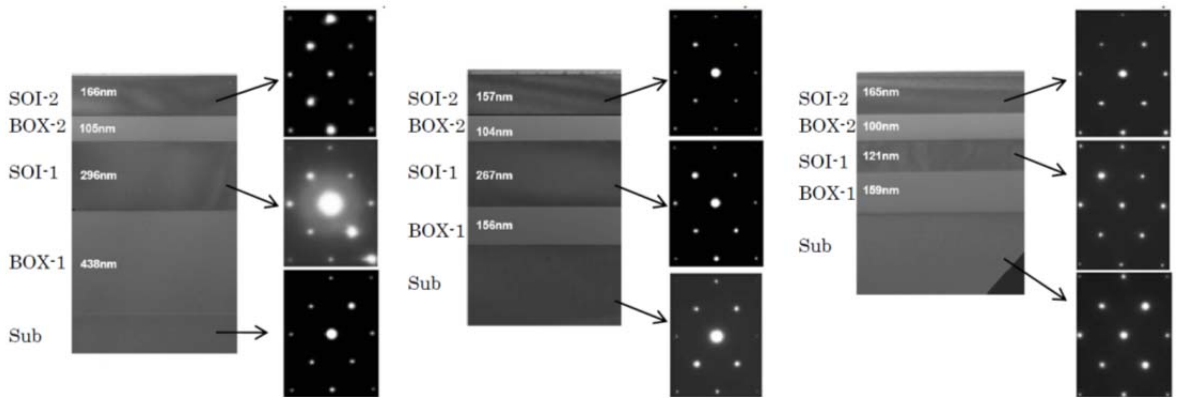
Three types of SOI substrates are used in this experiment. Substrate A: SOI substrate with 700nm of SOI thickness (=top silicon thickness) and 400nm of BOX thickness (= buried oxide thickness) made by SmartCut method at SOITEC, Substrate B: SOI substrate with 700nm of SOI thickness and 150nm of BOX thickness made by SIMOX method at Siltronic Japan, and Substrate C: SOI substrate with 550nm of SOI thickness and 150nm of BOX thickness made by SIMOX method at Siltronic Japan. In addition, normal bulk silicon substrate is used as a reference. SIMOX process (ion implantation and annealing) are adapted by 200mm size SIMOX mass production equipment at Siltronic Japan. SIMOX processes on four silicon substrate (3 SOI and 1 bulk) are implemented at same lot for scrutiny.

Because usual SOI thickness of SOI made by SIMOX with ITOX at Siltronic Japan is 175nm, additional epitaxial growth process is applied on substrate B and C to get 700nm and 550nm SOI thickness, respectively. Parameters and results of substrates are described in table 2-1.

2-7-3 Results of uniform SIMOX on flat SOI substrate

The cross sectional images and diffraction patterns of transmitted electron by transmission electron microscope (TEM) on substrate A, B, and C are shown in figure 2-13 (a) – (c). In these pictures, BOX-1 layer is the original BOX layer and BOX-2 layer is made by this experiment. SOI layer is separated into SOI-1 and SOI-2 by creation of BOX-2.

If there are defects in substrate, line shape contrast of pattern will be appeared in TEM images. If there are no disorders in silicon crystal structure, small bright points will be observed in the photograph of diffraction pattern of transmitted electron. The cross sectional images and diffraction pattern of transmitted electron by TEM can evaluate the quality of silicon layers stably.



(a) (b) (c)

Figure 2-13 Results of uniform SIMOX on flat SOI substrate
(a) Substrate A: 700nm-SOI and 400nm-BOX made by SOITEC
(b) Substrate B: 700nm-SOI and 150nm-BOX made by Siltronic Japan
(c) Substrate C: 550nm-SOI and 150nm-BOX made by Siltronic Japan

Additional evaluation by Secco Etching[65] which is one of the quantitative and destructive defect analysis is applied. The original method of Secco Etching was reported by F. Secco d' Aragona in 1972 as a defect evaluation method of silicon substrate. Because the original Secco Etching makes deep pits in silicon layer, it is difficult to evaluate thin silicon layer. Krause, Nakano, and Hemment reported modified evaluation method of Secco Etching[66-68] to evaluate SOI substrate. In this thesis, modified evaluation method of Secco Etching by Hemment[68] is applied in defect analysis as Siltronic Japan applies in mass production.

The results of quantitative and destructive defect analysis on SOI-1; silicon layer for CMOS electrical circuits and SOI-2; silicon layer for optical circuits are shown in table 2-1.

In ITRS (International Technology Roadmap for Semiconductors) published in 2011 corresponding to 22nm CMOS design rule, silicon substrate with defect density of less than 1.0 x $10^4/cm^2$ is regarded as extremely low defect level[69]. In actual design of electrical circuits, compensating circuit is generally prepared for a defect rescue as redundancy[70]. Regarding defect density of less than 1.0 x $10^4/cm^2$ as extremely low defect level shows a substrate with defect density of less than 1.0 x $10^4/cm^2$ has enough quality which does not require additional redundancy. So all substrates have adequate condition in surface silicon layer (SOI-2) for CMOS integrate circuits. Comparing to reference bulk silicon substrate, substrate A has extremely good quality in defect density.

Table 2-1 substrate parameters and results of defect density.

	parameters of substrates				results of defects density by Secco Etching	
	SOI manufacturer	process	thickness of BOX-1 (nm)	thickness of SOI (nm)	silicon layer for CMOS electrical circuits(/cm^2)	silicon layer for optical circuits(/cm^2)
A	SOITEC	Smartcut	400	700	1.8×10^3	$> 5 \times 10^7$
B	Siltronic Japan	SIMOX +Epi	150	700	1.6×10^4	$> 5 \times 10^7$
C	Siltronic Japan	SIMOX +Epi	150	550	2.0×10^4	$> 5 \times 10^7$
reference	Siltronic Japan	bulk			2.7×10^3	

From the cross sectional images and diffraction patterns of transmitted electron by transmission electron microscope (TEM), silicon layer for optical circuits (SOI-1) of substrate A has lower contract. This result shows lattice structure of silicon layer for optical circuits (SOI-1) of substrate A has larger distortion. By further TEM analysis on substrate A, threading dislocation was found as shown in figure 2-14. Although there is a threading dislocation in silicon layer for optical circuits (SOI-1), there is no dislocation in surface silicon layer for CMON electrical circuits (SOI-2). So, defects in SOI-1 and defects in SOI-2 can be regarded as independent. The result that the cross sectional image of diffraction pattern of SOI-1 in substrate A has lower contrast might attribute to that substrate A has thicker BOX-1 layer than substrate B or C.

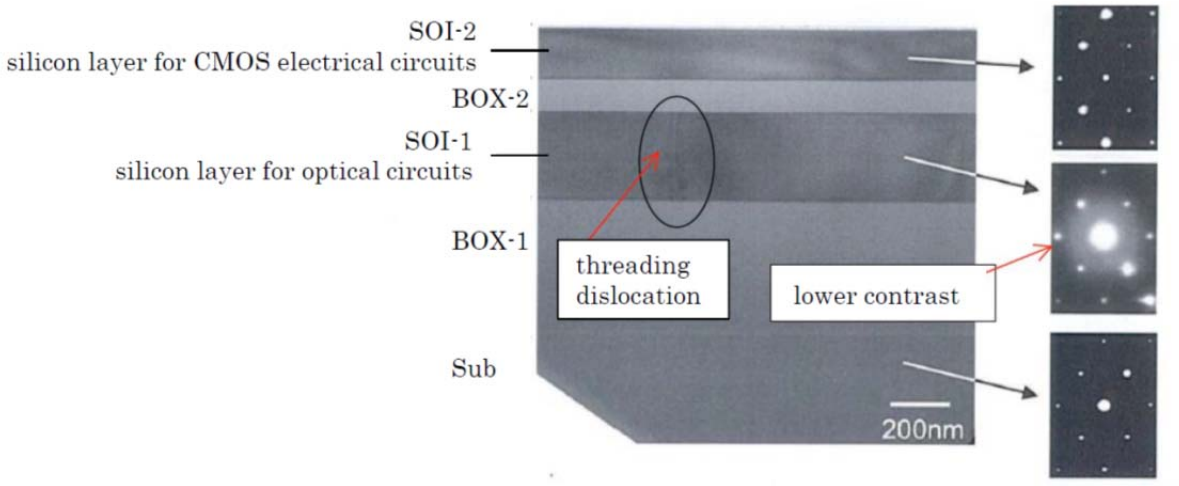


Figure 2-14 Cross sectional TEM images and diffraction pattern in substrate A.

The experiment of uniform SIMOX on flat SOI substrate in this section reveals that all substrates have adequate condition in surface silicon layer for CMOS integrate circuits (SOI-2) and some defects are created in silicon layer (SOI-1) for optical circuits (SOI-1).

In purchasing high-priced substrate such as SOI substrate, image of X-ray topography[70] which warrants there is no defect of the substrate with non-destructive way can be attached.

Because the distance between SOI-1 and SOI-2 is only 100nm or 150nm which is the thickness of BOX-2, it is impossible to warrant that there are no defects in SOI-2 with image by X-ray topography. The defect observation by optical microscope cannot easily distinguish a defect position in SOI-1 from a defect in SOI-2 because distance of 150nm or 200nm is less than focusing depth.

In order to commercialize EPIC in which CMOS electrical circuits and optical circuits are located on different silicon layer, development of non-destructive defect evaluation method of EPIC substrate is necessary which distinguish a defect in a silicon layer for CMOS electrical circuits, in a silicon layer for optical circuits, or supporting bulk silicon layer. And the non-destructive defect evaluation method of EPIC substrate is to be simplified method which can be adaptable for one hundred percent inspection.

2-8 Position of this research

In this research, a production method of SOI substrate which fabricates optical waveguide underneath the surface silicon layer is investigated as a critical technology for commercialization of EPIC. A non-destructive defect evaluation method of EPIC substrate which distinguishes defect among in a silicon layer for CMOS electrical circuits, in a silicon layer for optical circuits, or supporting bulk silicon layer is investigated as an essential technology to make CMOS electrical circuits on the surface silicon layer.

In addition, a memory device which utilizes interaction of SOI transistor and propagating light in optical waveguide underneath the transistor derived from the characteristics of making SOI transistor located immediately above the optical waveguide is investigated.

2-9 Summary

In this chapter, the possibility of pattern SIMOX process to fabricate an optical waveguide underneath the surface silicon layer as a silicon waveguide technology adaptable for CMOS integrated circuits is indicated. The pattern SIMOX process with transparent mask is proposed which avoids creating cracks or defects on surface silicon layer. By the experiment of uniform SIMOX on flat SOI substrate, the defect characteristics that the surface silicon layer has good quality in defect density and there are some defects in silicon layer for optical circuits, are shown. From the defect sensitivity that small defect does not affect property of optical circuits and affects property of CMOS electrical circuits, a simplified non-destructive defect evaluation method which detects the depth of defect position in 0.1micron resolution is required as an essential technology of EPIC.

Chapter 3 Non-destructive defect pinpointing by fluorescent microscope

3-1 Introduction

In EPIC substrate which consists of silicon layer for CMOS integrated circuits and silicon layer for optical circuits, an impact of defect depends on the layer where defect exists as shown in figure 3-1. From the experimental results in chapter 2 that defects exist in silicon layer for optical circuits beneath the surface silicon layer with no defect for CMOS circuits, necessity of non-destructive defect examination method which pinpoints the layer where defect exists is indicated.

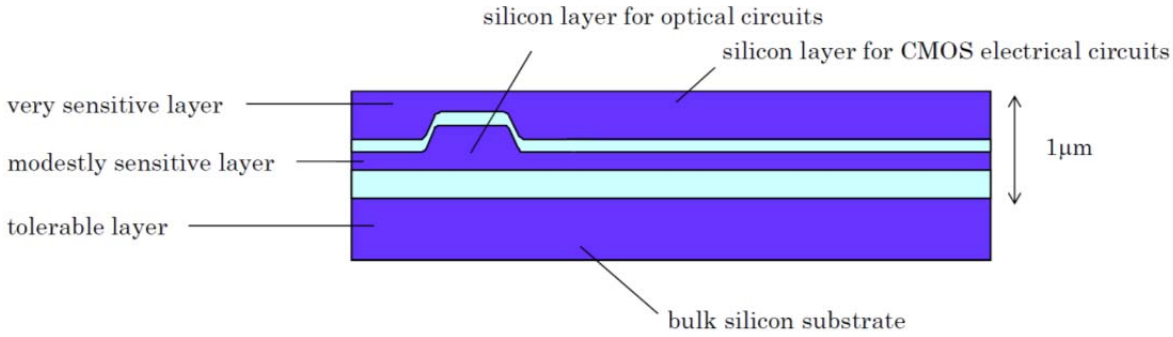


Figure 3-1 Various impact of defect depends on the layer where the defect exists

X-ray topography[71] has been used in an examination of bulk silicon substrates. X-ray topography indicates the defect without the depth information of the defect. Recently in the examination of SOI substrates, monitoring of UV reflecting laser light from the substrates [72] is used to detect the defects located in the surface region. Although this defect examination method with UV laser light can find defects in surface region non-destructively, this method cannot indicate the defect position in depth direction. Therefore this method cannot determine the defect existing silicon layer in EPIC substrate which consists of silicon layer for CMOS integrated circuits and silicon layer for optical circuits.

In this chapter, non-destructive defect examination method which can

pinpoint the defect with 30nm resolution in depth direction is described. After explanations of an existing defect examination method by fluorescent microscope and computational photography which is the basic technology of this research, proposed non-destructive defect pinpointing method is described. The validation result with pinpointing fluorescent beads on the substrate with 1μm-depth grooves is shown. In addition, method of expanding the measurement range and application of proposing non-destructive defect pinpointing method are discussed.

3-2 Existing defect examination method by fluorescent microscope

Nevin and Higgs reported the defect examination methods of SOI substrate using fluorescent microscope. [73, 74] Nevin excited defects with 532nm visible laser light and detected the photo-luminescent light with 827nm band emission filter. The fluorescent microsystem which Nevin used is shown in figure 3-2. Although both of exciting light and photo-luminescent light are opaque for silicon substrate, Nevin detected the defects in the depth range from 0μm to 4μm from the surface. [74]

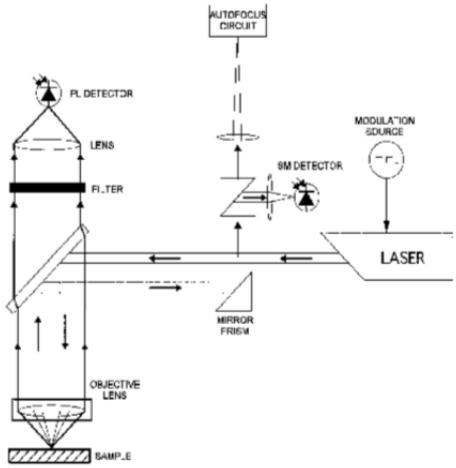


Figure 3-2 Fluorescent microsystem which Nevin used in defect examination [74] Wavelength of Exciting light and observing light are 532nm and 827nm, respectively.

The existing method of detecting the defect depth by fluorescent microscope is discussed. Because the brightness of a defect in fluorescent microscope reaches to the maximum brightness when focusing depth is set to defect position, it is necessary to measure the brightness of photo-luminescent light from a defect during varying the focusing position of the microscope to obtain the defect depth. After obtaining the relation between focusing position in depth direction of fluorescence microscope and brightness of photo-luminescence light from the defects, the position of the maximum brightness indicates the depth of defect as shown in figure 3-3.

In the case of automatic defect examination, image capturing with varying focusing depth and image analyzing of the captured images are performed at each XY position. For example, when defect examination is required to detect the defect in the range from surface to 2μm depth with a depth resolution of 0.1μm, image capturing with varying the focusing depth with 0.1μm step from the surface to 2μm depth. However higher NA objective lens is required to detect a defect sensitively, increasing the NA of objective lens reduces the observing area. For example, combination of x40/NA0.8 objective lens and 36mm x 24mm 2D imager with 6μm pixel size captures image area of 0.9mm x 0.6mm with 0.15μm/pixel resolution. When 300mm diameter silicon substrate examination with 20 images

in depth direction at each position is implemented, data size of captured images for one substrate reaches about 9TB even if image data is compressed to JPEG format. So less data size is required in examination with fluorescent microscope.

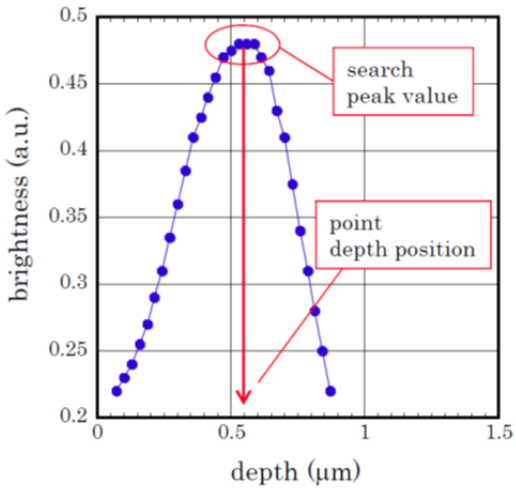


Figure 3-3 Defect pinpointing method with existing method

As 3D image capturing method with one shot by fluorescent microscope without changing focus position, there are applying spatial light modulator [75, 76], cylindrical lens [77], and quadratically-distorted grating [78]. But these methods reduce capturing area in inverse proportion to number of depth. So required data size in defect examination cannot be reduced.

3-3 Deblurring technology with computational photography

In the way of reducing the data size in fluorescent microscopy, deblurring technology with computational photography which creates focused image from blurred image is discussed. Mainstream of deblurring technology with computational photography are lightfield method [79], coded aperture method [80], and extended depth method [81]. Lightfield method is to create focused image by selecting pixel position of image which is captured with applying

microlens array in camera system. Coded aperture method is to synthesize the image of rapid moving target by removing blurring from multiple images captured with various apertures at fast rate. Extended depth method is to produce focused image from blurred image which is captured with moving of imager.

In consideration of applying for fluorescent microscope, lightfield method has a disadvantage in image resolution and coded aperture method is not suited for long exposure time imaging. Extended depth method is considered to be fitted for fluorescent microscope with moving of specimen instead of imager.

The concept of extended depth method is that production of focused image is possible if blurred condition is given. The camera system which Nayar performed extended depth [81] is shown in figure 3-4. Nayar moves image detector during exposure in focus direction. Figure 3-5 shows (a) captured image and (b) produced image. Figure 3-5(a) has blurring in all area because imager was moving during exposure. By analyzing blurring condition as a function of pixel position, focused image as shown in figure 3-5(b) was produced.

Extended depth method makes it possible to produce focused images of both targets in near position and targets in far position at the same exposure. So extended depth method is regarded as the method which can reduce image capturing number because this captures focused images of the targets which cannot be captured at the same exposure.

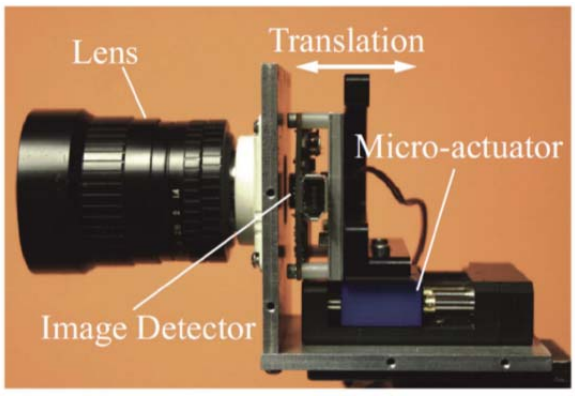


Figure 3-4 Camera system which Nayar performed extended depth [81]

(a) Captured Image (f/ 1.4, T=0.36sec) (b) Computed EDOF Image

Figure 3-5 Images of extended depth method by Nayar. [81]
(a) captured image (b) produced focused image

3-4 Proposed imaging method

The imaging target in this research is a defect in silicon substrate. From the experimental results in chapter 2, the densities of defects in silicon layer for CMOS electrical circuits and in silicon layer for optical circuits are less than 1.0 x 10^4/cm^2 and less than 5.0 x 10^7/cm^2, respectively. Image capturing area with the combination of x40 objective lens and full size imaging device (36mm x 24mm) is 0.9mm x 0.6mm. The number of defects in this image capturing area in silicon layer for CMOS electrical circuits and optical circuits are less than 5.40 x 10^1 and 2.7 x 10^5, respectively. Because these numbers are two digits smaller than the number of pixels in imager; 2.4 x 10^7, targets in captured image are sparse. There might be enough spaces around defect in captured image by fluorescent microscope. The author thought that there might be enough space for blurred image with depth information, and consequently image capturing number might be reduced.

The proposed method is described using the 3D space shown in figure 3-6. There are two target markers A and B between Z_{start} where is the start position of

exposure, for example the surface, and Z_{end} where is the end position of exposure, for example Z_{end} depth position from the surface. The position of marker A and B in depth direction are z_A and z_B, respectively. And both z_A and z_B are located between Z_{start} and Z_{end}, and z_A is located almost center of Z_{start} and Z_{end} and z_B is located near Z_{end}.

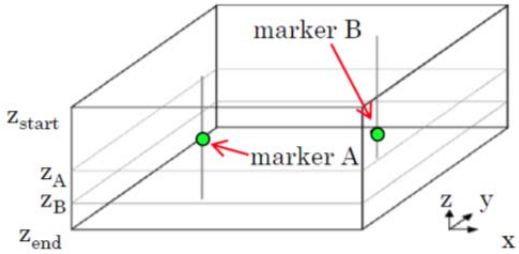


Figure 3-6 3D space for proposed method discussion

The proposed method is composed of following two exposure process.

The movements of mechanical stages of specimen in the first exposure are expressed in the equations from eq. 3-1 to eq. 3-3. X and y stages are fixed during exposure time: t ($0 \leq t \leq t_{ex}$) and z stage is moved from z_{start} to z_{end} at constant speed.

Figure 3-7(a) presents the movement of projected image of marker A on imaging devices, and figure 3-7(b) presents the recorded image. At the beginning of exposure (t=0) focus plane is not on marker A, and image of marker A on imaging device is defocused. At $t = 1/2t_{ex}$, focus plane is on marker A, and image of marker A on imaging device is focused, so image of marker A on imaging device has the maximum brightness and the smallest area. At the end of exposure ($t= t_{ex}$) focus plane is not on marker A, and image of marker A on imaging device is defocused. However the recorded images of marker A and B through the first exposure have blurring comparing to focused images, the x and y positions of marker A and B can be recognized because x and y stages are fixed. The first exposure step is to recognize x and y positions of the targets.

$$z(t) = z_{start} + (z_{end} - z_{start})\frac{t}{t_{ex}} \quad \text{(Eq. 3-1)}$$

$$x = x_0 \quad \text{(Eq. 3-2)}$$

$$y = y_0 \quad \text{(Eq. 3-3)}$$

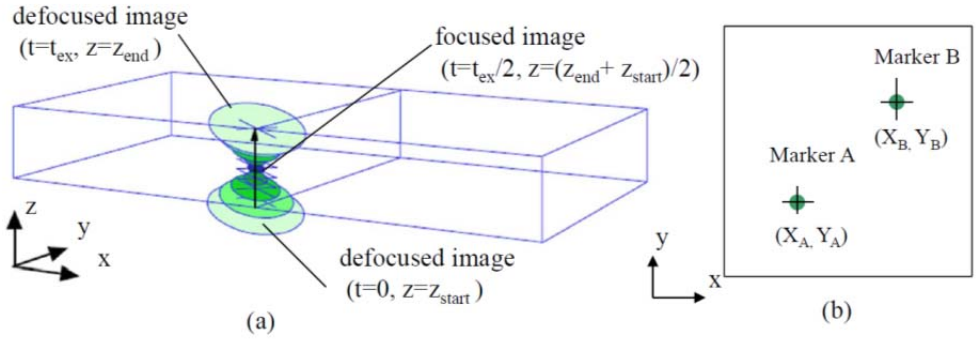


Figure 3-7 Description of the first exposure step of proposed method
(a) movements of projected image of marker A on imager (b) recorded image

The movements of mechanical stages of specimen in the second exposure are expressed in the equations from eq. 3-4 to eq. 3-6. Z stage is moved from z_{start} to z_{end} at constant speed as same as the first exposure. X and Y stages are moved synchronously on the circular track with radius L at constant angle velocity. Figure 3-8(a) presents the movement of projected image of marker A on imaging devices, and figure 3-8(b) presents the recorded image. At the beginning of exposure (t=0) focus plane is not on marker A, and image of marker A on imaging device is defocused. At $t = 1/2t_{ex}$, focus plane is on marker A, and image of marker A on imaging device is focused, so image of marker A on imaging device has the maximum brightness and the smallest area. At the end of exposure ($t= t_{ex}$) focus plane is not on marker A, and image of marker A on imaging device is defocused. Because x and y stages are moved synchronously with z stage in the second exposure, the projected image of marker A on imaging device is moved on the circular track with the radius of L multiplied with optical magnification of

microscope M. The recorded images of marker A and B expresses the circular movement of stages along with blurring information as shown in figure 3-8(b).

By the comparison of equations 3-2, 3-3 and 3-5, 3-6, the center of circular image of marker A and B in figure 3-8(b) is the position of image of marker A (X_A, Y_A) and B (X_B, Y_B) in figure 3-7(b). By drawing the lines from positions of marker A (X_A, Y_A) and B (X_B, Y_B) to the focused point of recorded circular images of marker A and B, θ presents the time when focus position is located at marker position. From the reason that z stage moves at constant speed, time focus position is located at marker position indicates the depth position. The second exposure step is to measure z positions of the targets.

Therefore 3D positions of marker A and B can be pinpointed by analyzing two images captured by proposed method.

$$z(t) = z_{start} + (z_{end} - z_{start})\frac{t}{t_{ex}} \qquad \text{(Eq. 3-4)}$$

$$x(t) = x_0 + L \times \cos\left(\pi \frac{t}{t_{ex}}\right) \qquad \text{(Eq. 3-5)}$$

$$y(t) = y_0 + L \times \sin\left(\pi \frac{t}{t_{ex}}\right) \qquad \text{(Eq. 3-6)}$$

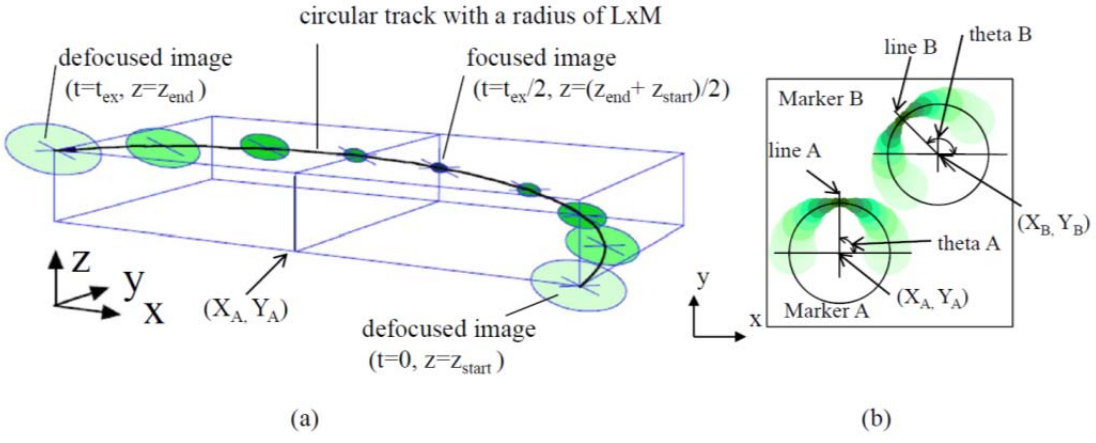


Figure 3-8 Description of the second exposure step of proposed method
(a) movements of projected image of marker A on imager (b) recorded image

3-5 Experiment for verification

The experiment for verification of proposed method to pinpoint 3D positions of marker by two exposure process is described.

In this experiment, fluorescent beads with uniform diameter are used to verify the accuracy of pinpointing depth.

3-5-1 Experimental setup and specimen

Experimental setup is shown in figure 3-9. An FOV type fluorescent microscope (Axio Imager Z1 made by Carl Zeiss) is used. A piezo type x and y stage (P-628K001 made by Physik Instrumente) and a piezo type z stage (P-622.ZCL made by Physik Instrumente) are placed on the specimen stage of the microscope to perform x, y, and z movement of specimen. X and y stage and z stage are controlled by closed loop system using x and y stage controller (E-710.4CL made by Physik Instrumente) and z stage controller (E-661CP made by Physik Instrumente), respectively. The target position of z stage is set by function generator synchronized with x and y stage controller. DSLR camera (Alpha 900 made by Sony Corporation) is attached to fluorescent microscope through 2.5x image conversion lens (Carl Zeiss). The DSLR camera has 24.81M pixels CMOS imager whose pixel size is 5.94μm. Both DSLR camera and x and y stage controller are directly controlled by PC.

The control signals for target position of x and y stage are sinus function and phases of these signal have difference of 90 degrees to get circular movement of specimen. The amplitude and frequency of sinus function are of 5μm and 0.2Hz, respectively, and specimen is moved on circular track of 5μm radius and its angle velocity is 72deg/sec. 20x objective lens (Plan-APOCHROMAT 20x/0.8, Carl Zeiss) is applied in the fluorescent microscope. The combination of 20x objective lens and 2.5x conversion and 36.2mm x 24.1mm 2D imager captures image area of 724 μm

x 482 μm. In addition, specimen moves on 5μm radius circular track, imaging area is reduced to 714 μm x 472 μm by this circular movement.

In case the speed of z stage is set to 3μm/sec and exposure time is set to 4sec, scanning distance in depth is 12μm. Although the specifications of position accuracy of x, y, and z stages are 10nm, position accuracy of z stage is about 50nm because of existence of 200kHz vibration measured by stage feedback signal.

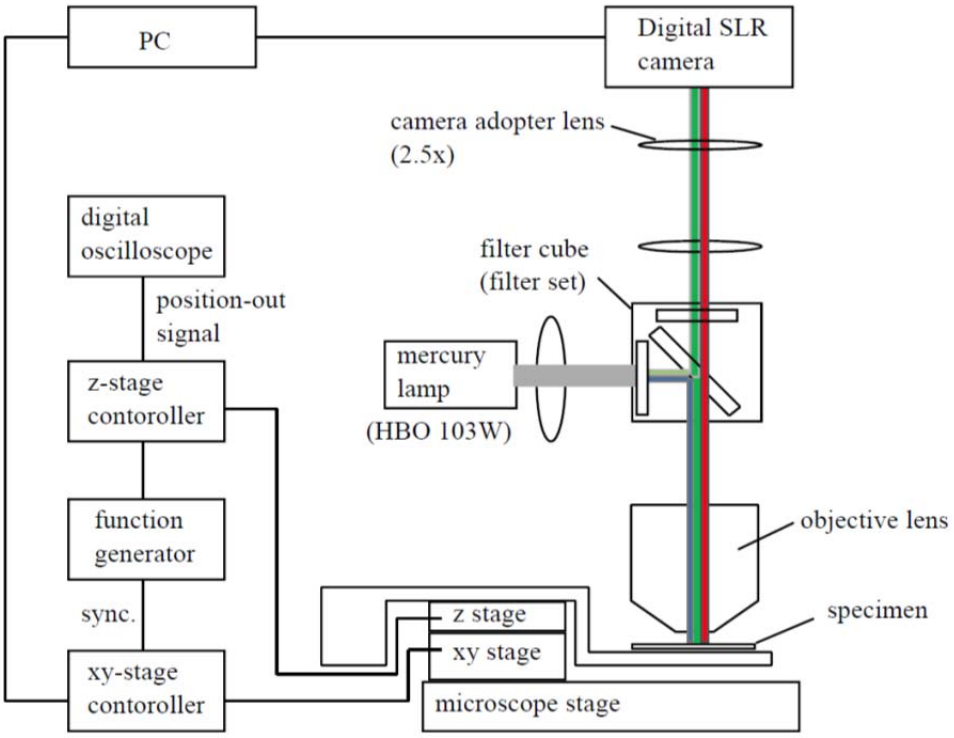


Figure 3-9 Experimental setup

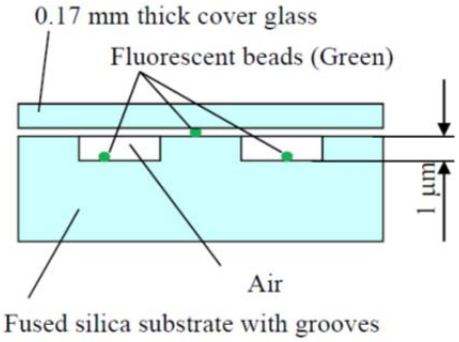


Figure 3-10 Specimen structure

A specimen structure is shown in figure 3-10. The material of substrate of specimen is fused silica and there are groove structures at the surface of substrate. A green color fluorescent beads of 0.3μm diameter (Fluoro-max G300 made by Thermo Fisher Scientific) are randomly placed on the substrate. A 0.17mm thick cover glass is placed because the objective lens is designed with 0.17mm cover glass. The depth of groove was 1.00μm measured by surface profile meter (P10 made by KLA Tencor).

3-5-2 Verification result

Obtained pictures are shown in figure 3-11. Emission filter of 525nm (No. 38, Carl Zeiss) wavelength is used at exposure in fluorescent microscope. Figure 3-11(a) is the picture by the first exposure step to pinpoint x and y positions of the targets. Figure 3-11(b) is the picture by the second exposure step to pinpoint z positions of the targets. The arrow in figure 3-11(b) indicates the direction which moves the specimen to objective lens. From figure 3-11(a) has enough contrast to pinpoint x and y positions of the targets.

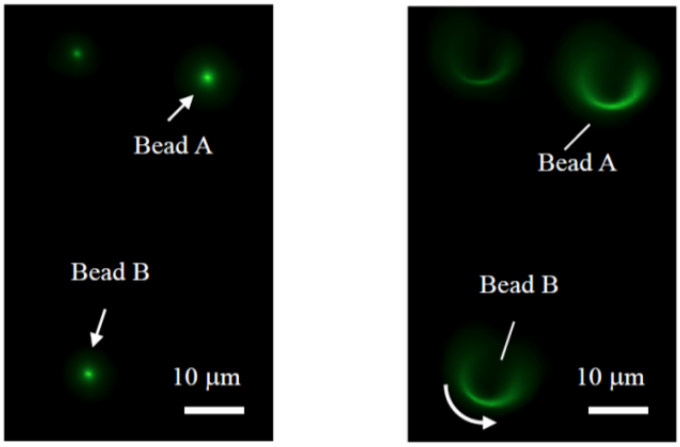


Figure 3-11 Pictures of the specimen by proposed method
(a) Picture by the first exposure to pinpoint x and y positions
(b) Picture by the second exposure to pinpoint z positions

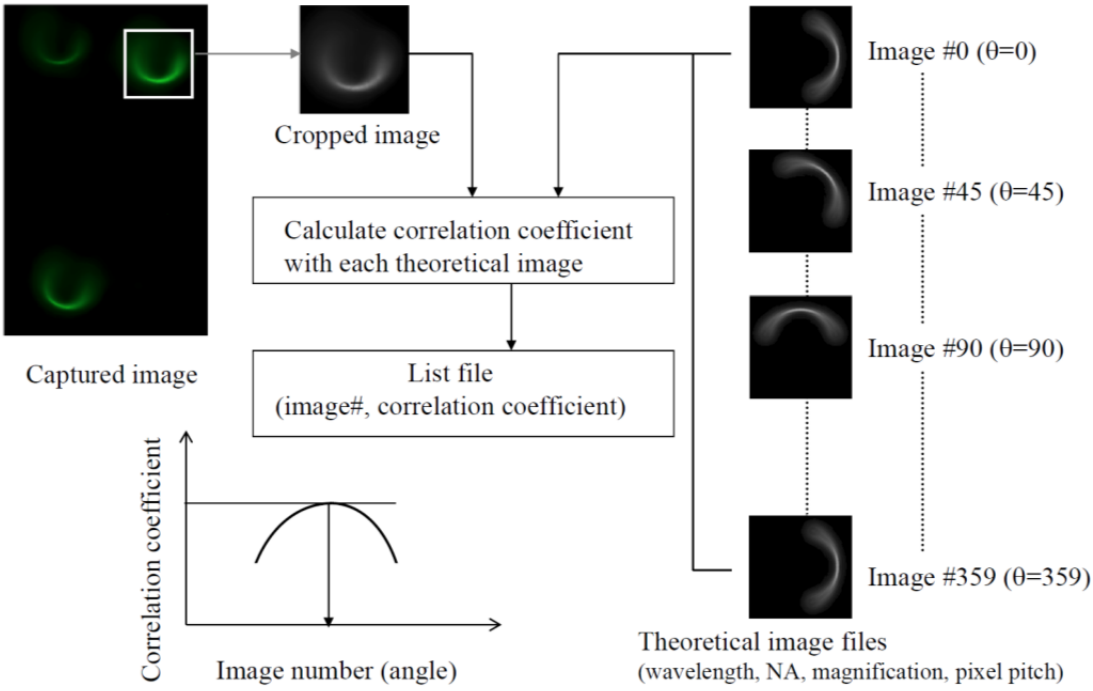


Figure 3-12 Algorithm for pinpointing z position

An algorithm for pinpointing the z position of markers with using figure 3-11(b) is shown in figure 3-12. First, theoretical image files are prepared with optical parameters of fluorescent microscope, wavelength of fluorescent

microscope, and stage moving parameters by Fourier optics [82]. 360 rotating with 1 degree step images (from #0 to #359) are prepared. Theoretical images are shown in right side in figure 3-12. These images from #0 to #359 correspond to -3μm to +3μm in z position. Next, image correlation coefficients between experimental image and each theoretical image are calculated. The image number with maximum correlation coefficient is searched, and the image number with maximum correlation coefficient is changed to the angle information. Using stage moving parameters angle information can be translated to z position information of the marker.

Figure 3-11 shows the calculation results of correlation coefficient between marker images A and B in figure 3-11(b) and theoretical images. In figure 3-11, the vertical axis is an arbitrary unit and horizontal unit is number of theoretical images used in correlation coefficient calculation. From this figure, there is a difference of 25 degrees between marker A and B. From the parameter of moving speed of 3μm/sec by z stage and 72deg/sec of angle velocity of circular moving by x and y stages, difference of 25 degrees corresponds to 1.04μm in depth difference which coincide with actual depth difference of 1.00μm between marker A and B. In addition the information of moving direction shown as arrow in figure 3-11(b), marker B is found to be closer to the objective lens than marker A, that is, marker A is indicated to be in the groove of the specimen.

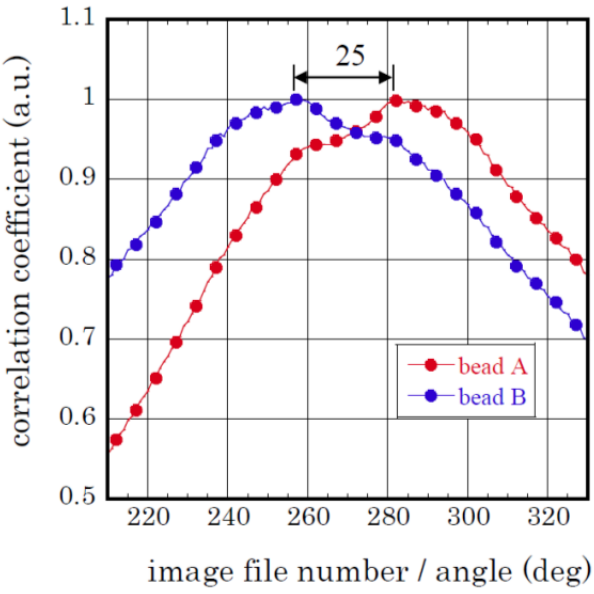


Figure 3-13 Calculation result of z position

Because increments of 1 degree calculation correspond to increments 0.04μm in depth position, the resolution of pinpointing the depth position of proposed method has less than 0.1μm. Although this proposed method has only two exposures, it has less than 1/10 of focusing depth of objectives in resolution of pinpointing the depth position. The depth range of theoretical images is from -3μm to +3μm, there is some degradation with 3μm in both ends of scanning range, so center of 6μm in scanning range has resolution of less than 0.1μm in pinpointing the depth position. Despite requiring 61 exposures in image capturing of 6μm range with 0.1μm step, the proposed pinpointing method is very effective.

In case this verification result applies to defect detecting in silicon substrates, pinpointing depth with less than 30nm resolution has been obtained in the range of more than 1.7μm. These resolution and range condition covers the required depth range of defect detection shown in figure 3-1.

However blurred image without overlapping is used in the above description, handling procedure of blurred image with overlapping is shown in figure 3-14.

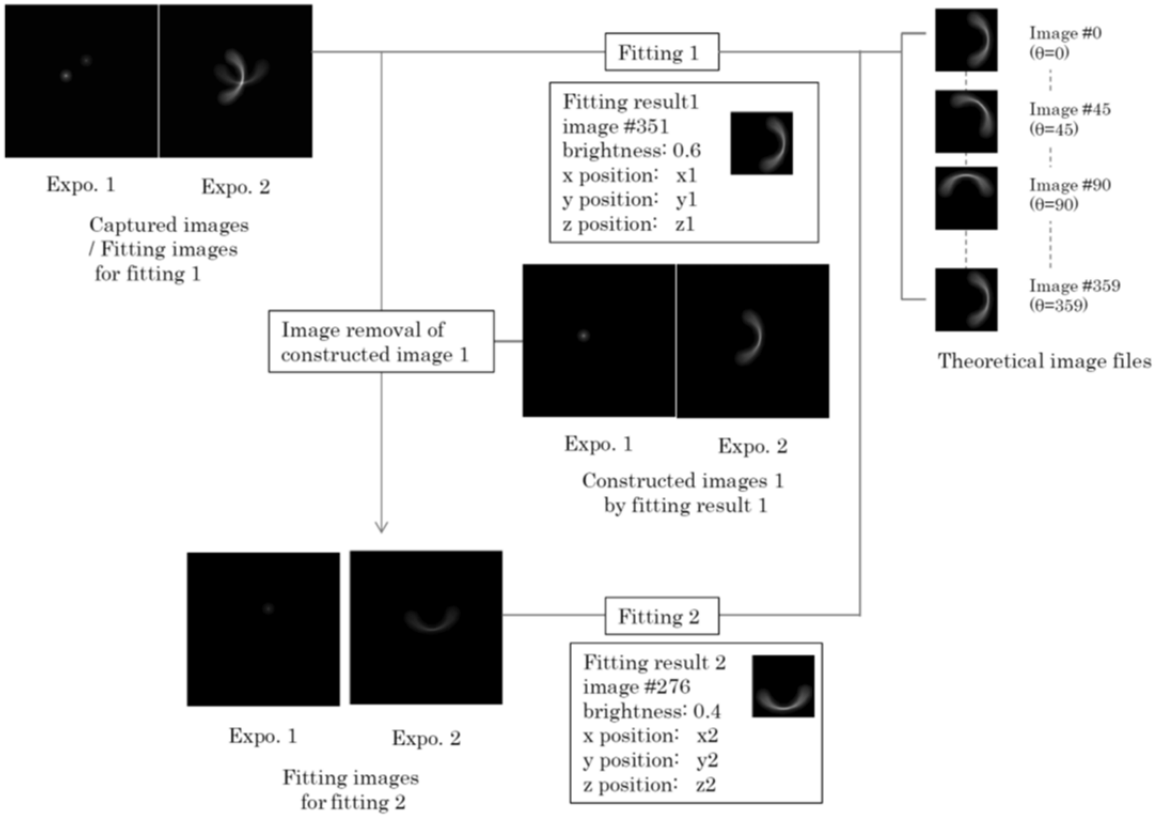


Figure 3-14 Algorithm for pinpointing z position in case image with overlapping

In figure 3-14, expo. 2 captured image in second exposure has overlapping. The same theoretical images shown in figure 3-12 are prepared for calculation of image correlation coefficient. The same procedures of calculation of image correlation between captured image and theoretical images are performed and obtain fitting result 1 in order to have position information and brightness data of the first marker. Next construct images of expo. 1 and expo. 2 with position information and brightness data of the first marker (fitting result 1) and construct the image of fitting images of expo. 1 and expo. 2 by removing construct images of expo. 1 and expo. 2 from captured images of expo. 1 and expo. 2. And second pinpointing procedures are performed to these construct images of expo. 1 and expo. 2 to pinpoint the position of the second marker.

The case when two blurred images are overlapped is discussed in figure 3-14. The same procedure of removing the constructed images by fitting result of

marker position and brightness from exposure images can be applied in the case when more than 3 images of marker are overlapped. Although two markers are assumed to be independent point shape markers in figure 3-14, this algorithm can be applied to not only point shape markers and also line shape markers and group of points shape markers. This application shows that proposed method can be used in pinpointing not only point defects and also threading dislocations.

3-6 Scanning range and expanding method of scanning range

Because this proposed defect detecting method involves moving of focus lens in exposure, thickness of cover glass is changed in exposure. The only slight change of thickness is non-negligible for spherical aberration under the huge index of 3.5 of silicon. From the viewpoint of tolerance in spherical aberration, applicable scanning range of proposed pinpointing method and expanding method of scanning range are discussed in this section.

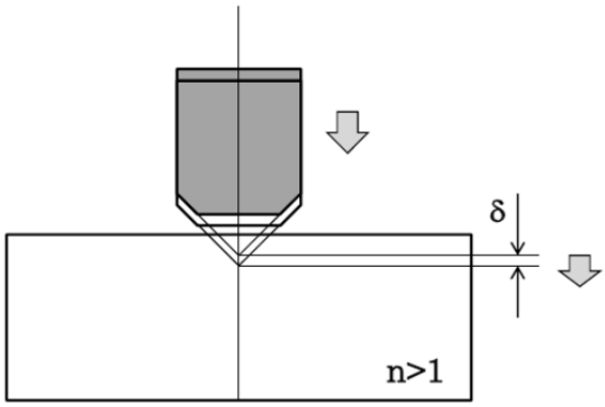


Figure 3-15 Thickness change of cover glass in exposure

3-6-1 Applicable scanning range of proposed pinpointing method

The amount of degradation in optics is usually expressed in rms which indicates precision of imaging when there is production error or deviation from designed environment. [83, 84] In the field of optical data storage, there are many report regarding influences of spherical aberration caused by thickness change in precision of imaging. The allowed spherical aberration in optical storage system was reported to 0.08λ rms by Yamamoto [83] and reported to 0.06λ rms by Ichimura [84]. In this chapter, 0.06λ rms is applied as a criterion of allowed spherical aberration to calculate applicable scanning range.

In Bluray optical disk system whose NA and wavelength are 0.85 and 405nm, respectively, Ichimura reported allowed thickness error of cover glass (n=1.5) is 5μm corresponding to allowed spherical aberration of 0.06λ rms [84]. Because spherical aberration brought from thickness error of cover glass is reversely proportional to wavelength and is proportional to 4^{th} power of NA [85], allowed thickness error of cover glass is 5.58μm at Navin's experimental condition to find defects in silicon (n=3.5) with NA0.8 objective lens at wavelength of 827nm [74]. Using with objective lens of 0.8 NA optimized at 0μm cover glass, applicable scanning range for defect observation is 0μm to 5.58μm from the surface without degradation by spherical aberration.

From the reason that spherical aberration brought from thickness error of cover glass is proportional to 4^{th} power of NA, applicable scanning range is reduced to 1.06μm when NA1.2 objective lens is used. Therefore in case bright objective lens (higher NA objective lens) is ideal, expanding method of scanning range is required.

3-6-2 Expanding scanning range with liquid-crystal panel

As a method of compensate spherical aberration caused by thickness error of cover glass, liquid-crystal panel is used [86, 87]. Figure 3-16 shows the liquid-crystal panel by Ohtaki [87]. This panel utilizes the effect that index change of Nematic-type liquid-crystal. By applying optimized voltages on each triple concentric electrodes of panel, approximate index profile of spherical aberration is created in liquid-crystal panel. Figure 3-17 shows the phase of optical ray passing through the liquid-crystal panel. Because the liquid-crystal panel has parallel surfaces, direction of optical ray is not changed without refraction, but phase distribution is caused according to index profile of liquid-crystal panel. It is possible to compensate the spherical aberration cause by thickness error of cover glass by applying phase distribution to cancel the spherical aberration on incident optical ray of objective lens.

The principle of expanding the scanning range of defect pinpointing with using liquid-crystal panel which compensate spherical aberration caused by thickness error is described. Figure 3-18(a) explains the relation between designed thickness cover glass thickness for objective lens and thickness margin which satisfy a criterion of allowed spherical aberration without spherical aberration compensating liquid-crystal panel. When using objective lens whose designed cover glass thickness is t_{cg}, focus point at the depth of t_{cg} is clearly focused with the minimum aberration. Focus point in the range of t_{margin} is focused within allowed spherical aberration. In case NA of objective lens is 0.85 and wavelength is 405nm in n=1.5 medium, thickness error of 5μm corresponds to a criterion of spherical aberration of 0.06λ rms, so width of t_{margin} is 10μm. Figure 3-18(b) explains that adequate focus point is not focused outside the range of t_{margin} because spherical aberration caused by thickness error excesses a criterion of spherical aberration of 0.06λ rms. Figure 3-18(c) explains that adequate focus point is focused outside the range of t_{margin} by applying liquid-crystal panel which compensates spherical aberration caused by thickness error. In case NA of

objective lens is 0.85 and wavelength is 405nm in n=1.5 medium, spherical aberration error caused by thickness error of 25μm (=t_{LCD}) can be compensated with liquid-crystal panel which create 2.8λ of 3rd order spherical aberration [86]. Therefore thickness margin of this system with liquid-crystal panel is expanded from t_{margin} (10μm) to t_{margin} + t_{LCD} (35μm). The compensating the thickness aberration can be done with in msec because there is no mechanical moving device in liquid-crystal panel.

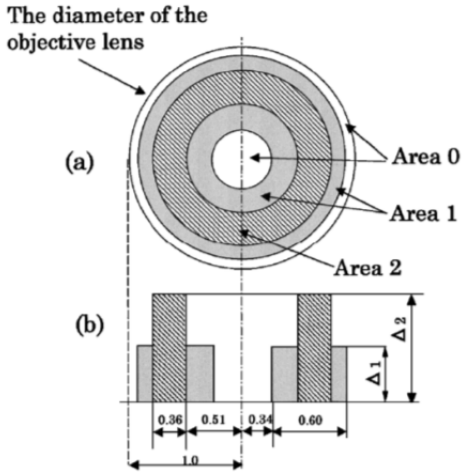


Figure 3-16 Liquid-crystal panel by Ohtaki [87]

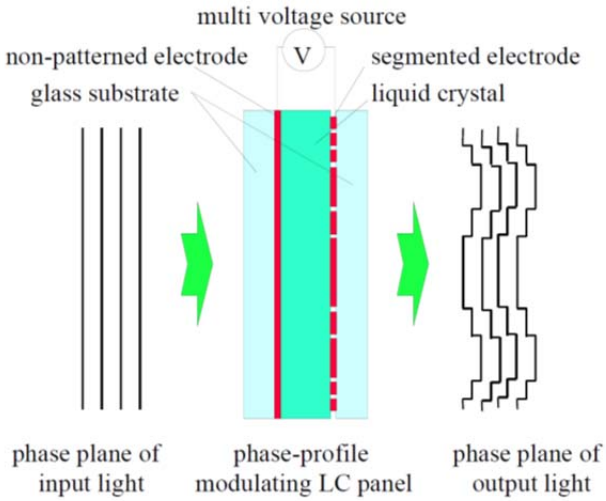


Figure 3-17 Phase profile of optical ray

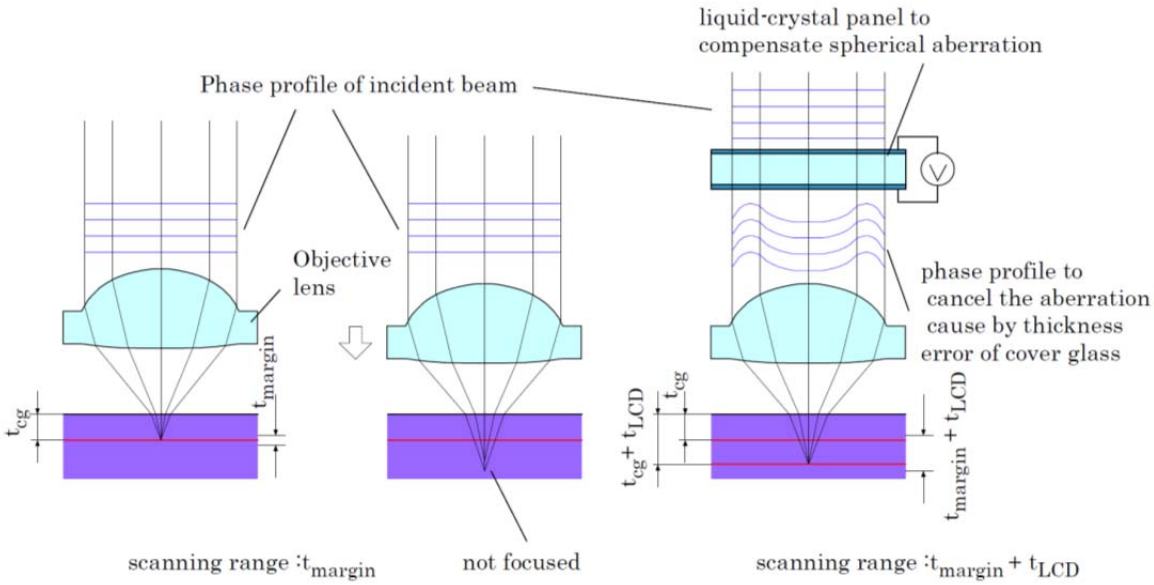


Figure 3-18 Principles of expanding scanning range by liquid-crystal panel

(a) Adequate focus point is focused at the designed depth

(b) Adequate focus point is not focused outside the range of t_{margin}

(c) Adequate focus point is focused outside the range of t_{margin} by liquid-crystal panel.

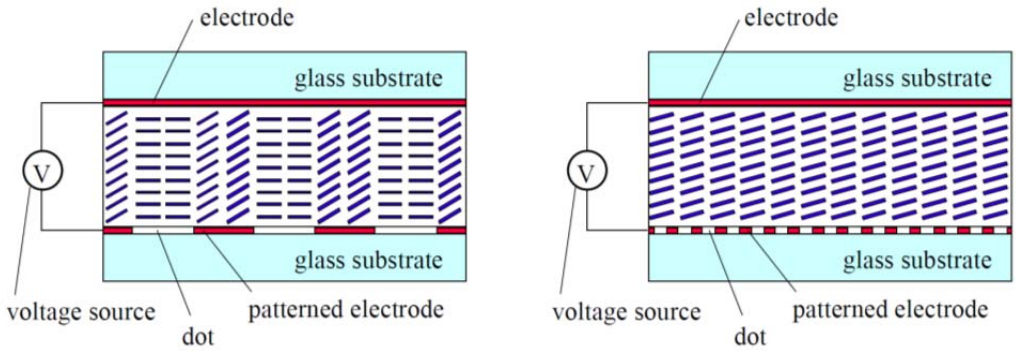
3-6-3 Proposed liquid-crystal panel for compensating spherical aberration

Because the liquid-crystal panel shown in figure 3-16 has concentric electrode and creates approximated phase distribution to three values, residual aberration is not negligible when amount of compensating spherical aberration is large. In addition the diffraction caused from rapid index change appears at boundary of electrodes. Considering these disadvantages, liquid-crystal panel which creates continuous index profile is proposed and is proved to be effective for expanding the scanning range.

Figure 3-19 explains the difference of electrode structure between existing liquid-crystal panel and proposed liquid-crystal panel. Figure 3-19(a) shows width of electrode in existing liquid-crystal panel is large. The movement of liquid-crystal molecular follows the shape of electrode and amplitude of the

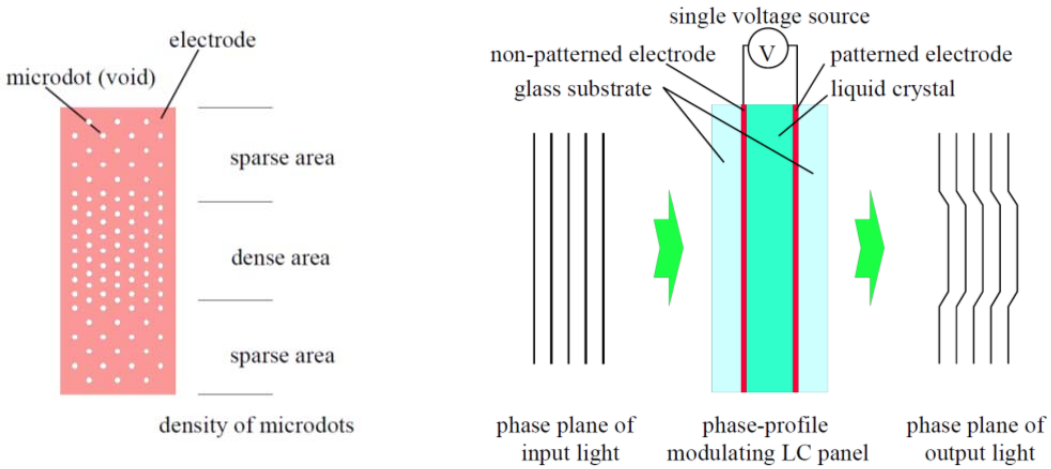
movement corresponds to the voltage applied to electrode. Figure 3-19(b) shows there are many small patterns on the electrode of proposed liquid-crystal panel. The size of pattern on the electrode is smaller than the area that liquid-crystal can follow, so amplitude of the movement of liquid-crystal corresponds to the average voltage applied to electrode.

Figure 3-20 shows the structure of liquid-crystal panel for compensating the spherical aberration consists of proposed liquid-crystal panel. As shown in figure 3-20(a), many microdots (voids) are fabricated on the electrode, and density of microdots is modulated and controls the amplitude of movement of liquid crystal. Therefore movement of liquid crystal at dense microdots area is smaller than movement of liquid crystal at sparse microdots area because the average voltage is smaller. Increasing the density of microdots in proposed liquid-crystal panel and decreasing applied voltage in existing liquid-crystal panel produce a similar effect. Although applying voltage is uniform in the panel, phase of optical ray passing though the panel has modulated profile corresponding to the density profile of microdots on electrode as shown in figure 3-20(b). The proposed liquid-crystal panel provides continuous phase profile by continuous density modulation of microdots.



(a) (b)

Figure 3-19 Existing liquid-crystal panel and proposed liquid-crystal panel
(a) movement of existing liquid crystal follows the shape of electrode and amplitude of the movement corresponds to the voltage applied to electrode
(b) movement of proposed liquid-crystal corresponds to the average voltage applied to electrode



(a) (b)

Figure 3-20 Principle of phase modulation in proposed liquid-crystal panel
(a) modulation profile of microdots density
(b) phase profile of passing optical ray of proposed liquid-crystal panel

3-6-4 Experiment of phase modulation with proposed liquid-crystal panel

The device structure for verification experiment is illustrated in figure 3-21. 8nm thick ITO transparent electrodes films are coated on 0.25mm polished glass substrates. Microdots with ϕ3μm, ϕ6μm, and ϕ12μm are fabricated on the electrode at one side of electrode. Polyimide alignment films are coated on the electrodes to align the direction of liquid crystal. Thickness of liquid crystal is set to 6μm. In order to investigate the effect of diffraction sensitively, laser light with 405nm wavelength is applied. The profile of applied voltage is rectangular wave of 5kHz and its average voltage is 0V, and the amplitude in the positive region is referred to representative voltage in the same manner of previous report [86, 87] as shown in figure 3-22.

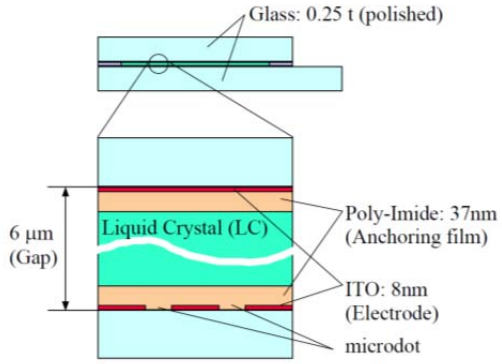


Figure 3-21
Device structure of liquid-crystal panel

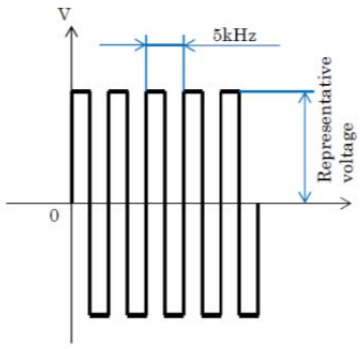


Figure 3-22
Profile of applied voltage

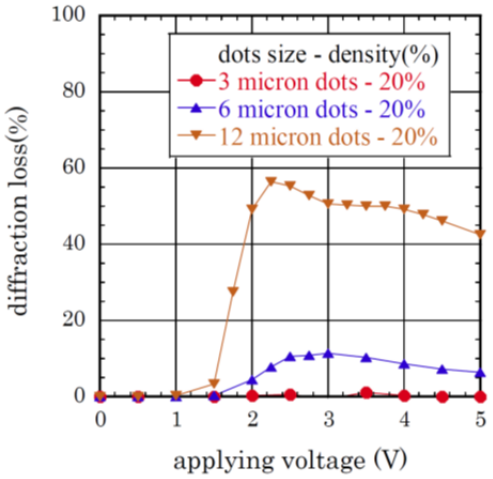


Figure 3-23
Results of diffraction loss

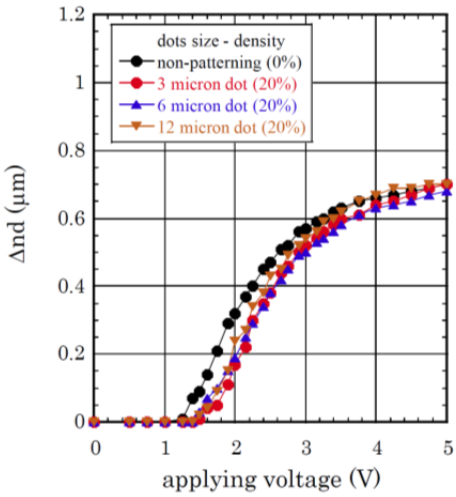


Figure 3-24
Results of phase retardation

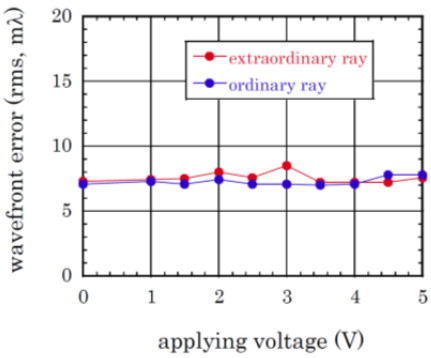


Figure 3-25 Wavefront error (beam quality) of the panel with microdots of ϕ3μm

In this proposal, it is important that the size of microdots is enough small and movement of liquid-crystal corresponds to the average voltage applied to electrode. The diffraction losses of liquid-crystal panels which have microdots of ϕ3μm, ϕ6μm, and ϕ12μm are fabricated on the electrode are measured. In the experiment, ϕ3mm beam with 405nm laser light is entered to the panel. And by placing the combination of f=50mm lens and ϕ0.2mm pinhole to passing beam, diffracted light is rejected at the pinhole. The light passing through the pinhole is measured by optical power meter. Figure 3-23 shows the experimental results of diffraction loss when the density of microdots is 20%. In these experiments the density of microdots is defined the area of microdots (voids). From this result, there is no diffraction loss on the panel with microdots of ϕ3μm, and there are diffraction losses on the panel with microdots of ϕ6μm and ϕ12μm. Although the number of microdots on the panel with microdots of ϕ3μm is the maximum at uniform density condition, there is no diffraction loss on the panel with microdots of ϕ3μm.

The experiment results of phase retardation with using same specimen with diffraction experiments are shown in figure 3-24. The method of phase retardation measurement is referred to the method with using quarter wavelength plate reported by Lee [88]. From this result all liquid-crystal panels with microdots on electrode have smaller movement of liquid crystal comparing to liquid-crystal panel without microdots. In the aspect of movement of liquid crystal, the applied voltage on the electrode with microdots is proved to be effectively decreased by fabricating the microdots.

The measured wavefront error (beam quality) of the panel with 20% density microdots of ϕ3μm at 405nm wavelength with the interferometer (DVD-400, Zygo Corporation) is shown in figure 3-25. The wavefront error is kept at less than 10mλ rms in all voltage regions. So there are no degradations even in the range liquid crystal is moved by applied voltage.

From the results of figure 3-23, 3-24, and 3-25, the panel with microdots of ϕ3μm creates uniform index change with no diffraction and no beam degradation.

The amount of phase retardation is reduced by fabricating microdots of ϕ3μm on electrode. The principle of proposed liquid-crystal panel shown in figure 3-20 is verified with the condition of microdots diameter of ϕ3μm.

3-6-5 Panel for compensating spherical aberration with proposed principles

In order to verify the creation of spherical aberration profile, a liquid-crystal panel with ϕ3μm microdots on electrode whose density is concentrically modulated to 16 grades from 3% to 76% as shown in figure 3-26. The phase profiles at the voltage conditions of 2.00V, 2.25V, 2.75V, and 3.25V are shown in figure 3-27. The phase profiles are measured at 405nm wavelength with the interferometer (DVD-400, Zygo Corporation). The created spherical aberrations are plotted in figure 3-28. From these results, the phase profiles of spherical aberration corresponding to the modulation profile of density of ϕ3μm microdots on electrode is proved and the amount of 1.5λ at 405nm wavelength is obtained at the applied voltage of 3V.

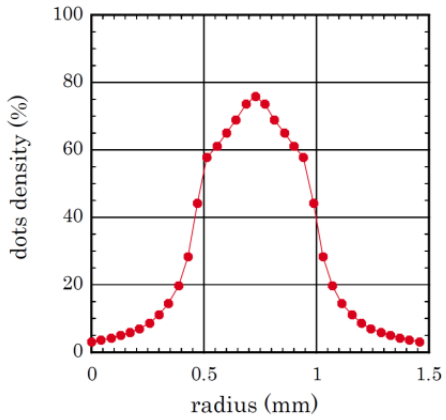


Figure 3-26 Density of microdots for spherical aberration profile

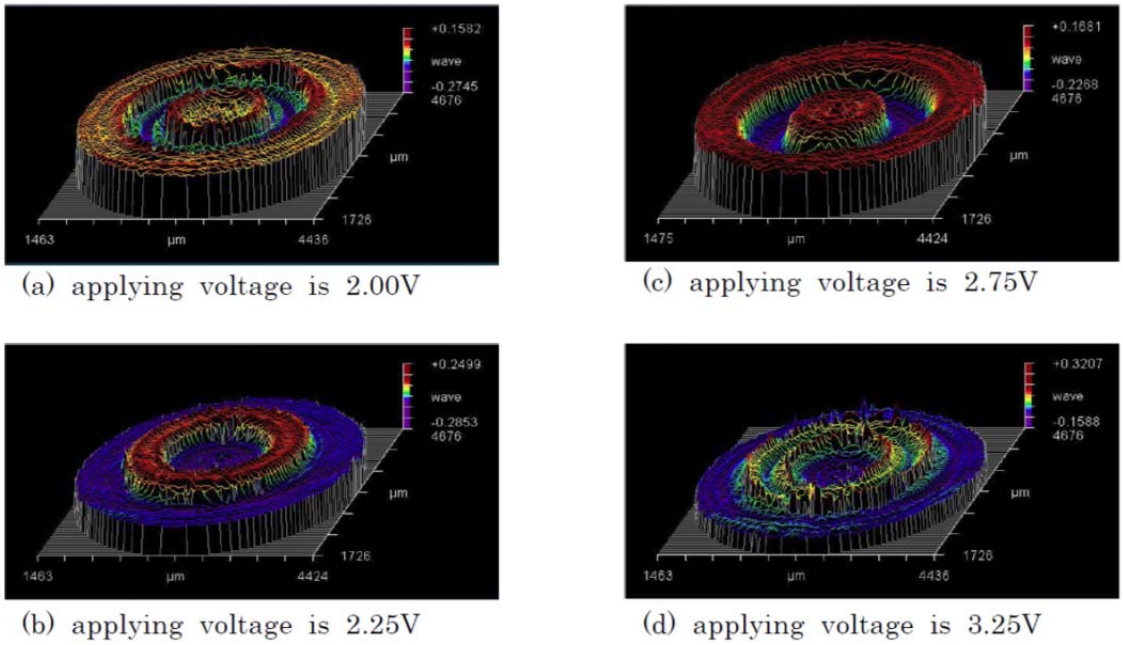


Figure 3-27 Measured phase profile of the panel

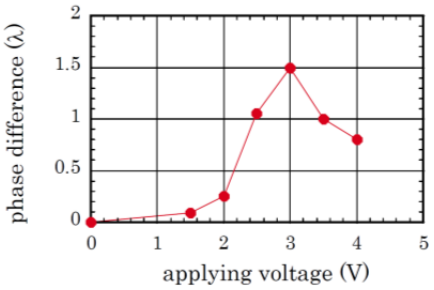


Figure 3-28 Created spherical aberration

3-6-6 Amount of expanding scanning range by proposed liquid-crystal panel

The amount of spherical aberration of 1.5λ at 405nm wavelength is equal to the amount of spherical aberration of 0.73λ at 827nm wavelength. The liquid-crystal panel which creates spherical aberration of 0.73λ compensates the spherical aberration caused by thickness error of 7.31μm and 1.44μm in n=3.5 silicon material with using objective lens of NA0.8 and NA1.2, respectively.

Under a criterion that allowed spherical aberration is 0.06λrms,

applicable scanning ranges of 7.31μm and 1.06μm with using objective lens of NA0.8 and NA1.2 are expanded to 12.89μm and 2.50μm, respectively. Therefore defect detection with objective lens of NA1.2 reaches the silicon in bulk silicon substrate under the BOX layer.

3-7 Application of non-destructive defect examination method

In this section, the applications of non-destructive defect examination method with fluorescent microscope to other fields are described.

3-7-1 Measurement of chromatic aberration of optics

The result of application in measurement of chromatic aberration of fluorescent microscope with proposed non-destructive defect examination method is described. The chromatic aberration is the effect that focusing points are varied with observing wavelength brought from the phenomena that index of lens material is not uniform to the wavelength. Although in the field of objective lens design, the combination of positive dispersion material which has smaller index at longer wavelength and negative dispersion material which has larger index at longer wavelength reduces chromatic aberration, there is residual chromatic aberration in actual range of use.

The markers on a same plane which emit different wavelength are observed at the same depth plane if there is no chromatic aberration in optics. When the markers on a same plane which emit different wavelength are observed at different depth, the measured different of depth indicates the chromatic aberration.

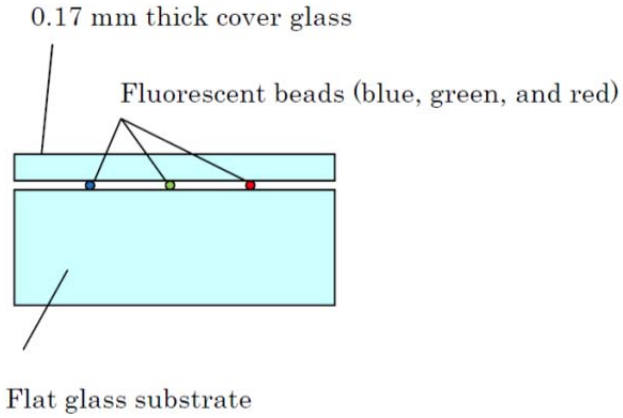


Figure 3-29 Specimen for measuring chromatic aberration

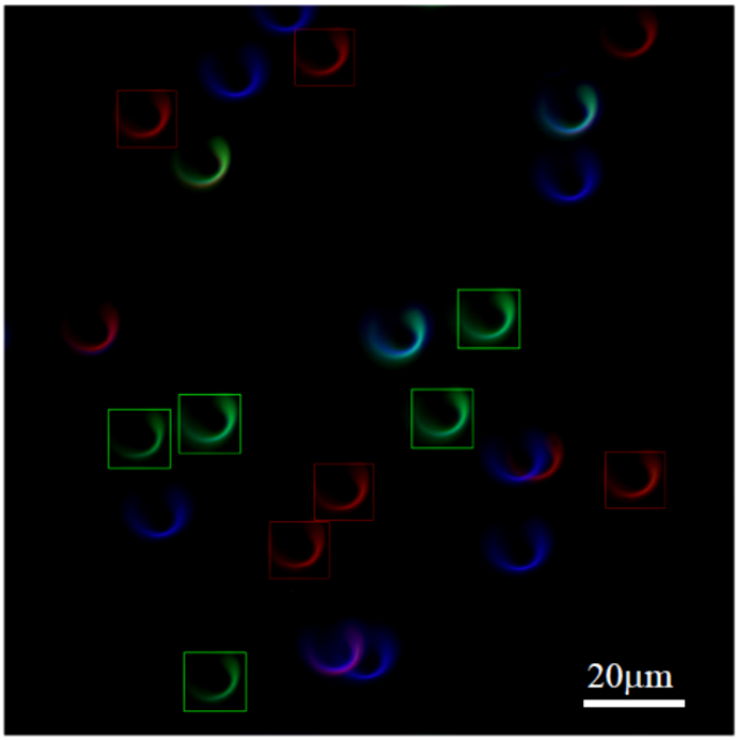


Figure 3-30 Captured image of chromatic aberration experiment

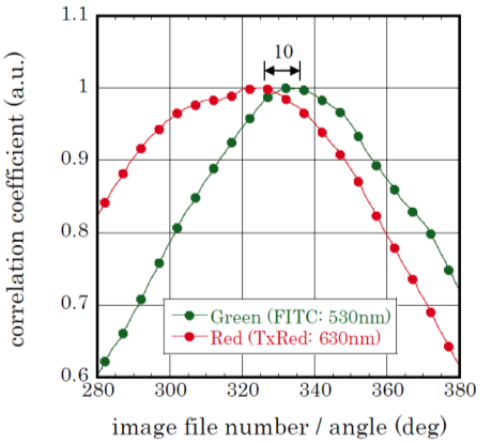


Figure 3-31 Result of chromatin aberration

A specimen for measuring chromatic aberration is illustrated in figure 3-29. Multiple 3 kinds of fluorescent beads (B300, G300, and R300 by Thermo Fisher Scientific) which emit blue, green, and red fluorescent wavelength and 0.17mm thick cover glass are placed on a flat glass substrate. This specimen is employed to the experimental setup shown in figure 3-9. The captured image by the same exposure condition with verification experiment described in section 3-5 is shown in figure 3-30. In this experiment No. 25HE triple band filter cube by Carl Zeiss is used to capture multi wavelength image coinstantaneously. A 40x objective lens of EC Plan-NEOFLUAR 40x/0.75, Carl Zeiss is used. The center wavelengths of the filter cube are designed to 460nm, 530nm, and 630nm for the detection of DAPI, FITC, and TxRed, respectively.

The highlighted images of 5 green and 5 red markers in figure 3-30 are implemented to pinpointing depth position procedure described in figure 3-12. The average calculation results of correlation coefficient are plotted in figure 3-31. In the calculation of correlation coefficient, theoretical images are provided with image calculation with 530nm (FITC) and 630nm (TxRed). The difference of 10 degrees is observed in figure 3-31 and there is 0.42μm corresponding 10 degrees in chromatic aberration between 530nm (FITC) and 630nm (TxRed) in used 40x objective lens (EC Plan-NEOFLUAR 40x/0.75, Carl Zeiss). This result presents the application of non-destructive defect examination method with fluorescent

microscope to measurement of chromatic aberration.

The method of chromatic aberration measurement with single image capturing has the merit of speedy measurement and simple recording the result with single image. The data of chromatic aberration is demanded in many cases with using multicolor observation including the following application. It is valuable to provide simple method to measure chromatic aberration.

3-7-2 Measurement of 3D position of gene and distance between genes

In the field of cancer diagnosis and drag discovery, FISH (Fluorescence in situ hybridization) [89, 90] is used to analyze genetic information of cells. In FISH method, target gene is marked by fluorescent marker and position of target gene becomes observable with fluorescent microscope. There are many researches to analyze mutations of cells [91] by 3D observation of gene position.

The occurrence frequency of translocation mutation of gene in cells is reported to be inversely proportional to the distance between genes [92], the necessity of measurement of 3D position of genes is increasing.

The application of non-destructive defect examination method with fluorescent microscope to measurement of 3D positions of gene and measurement the distance of genes is described.

The specimen with MRC-5 human lung tissue cell lines [93] is prepared and FISH stained with UroVysion staining kit [94] for bladder cancer diagnosis. There are four color fluorescent markers in the staining kit. Among four markers, Spectrum Red a red fluorescent marker hybridized to #3 chromosomes and Spectrum Green a green fluorescent marker hybridized to #7 chromosomes are used in this experiment.

A dual band fluorescent filter sets (#51006, Chroma technology Corporation) is used in the experimental setup shown in figure 3-9. The wavelength allocation of this cube is 530nm for FITC and Spectrum Green and

630nm for TxRed and Spectrum Red. The objective lens of EC Plan-NEOFLUAR 40x/0.75, Carl Zeiss is used and the chromatic aberration of this objective lens is reported in the previous section.

Figure 3-32 shows the captured images. Figure 3-32(a) is image of cell captured by the first exposure to pinpoint x and y positions. Figure 3-32(b) is image of cell captured by the second exposure to pinpoint z position. Figure 3-32(c) is reference image captured when x, y, and z stages are fixed. In this experiment two marked fluorescent markers in figure 3-21(a) are implemented to measure 3D distance because they are in close in x and y positions.

The distance in x and y positions are measured with figure 3-32(a) to 0.96μm. In order to pinpoint z positions of two markers, color separation of green and red process is implemented to figure 3-32(b). Figure 3-33(b) is image of red channel with #3 chromosome information separated from cropped image of figure 3-33(a). Figure 3-33(c) is image of green channel with #7 chromosome information separated from cropped image of figure 3-33(a). The calculation results of correlation coefficient process shown in figure 3-12 in figure 3-34. This figure indicates that there are 14degrees corresponding to 0.58μm difference in the z position between #3 chromosome and #7 chromosome. Considering the previous result of chromatic aberration of 0.42μm between 530nm green and 630nm red at used objective lens, the actual distance in z direction is revealed to 0.16μm.

Using the measured distance between #3 chromosome and #7 chromosome of 0.96μm and 0.16μm in x-y and z directions, respectively, the 3D distance between them is obtained to be 0.97μm.

The method of distance measurement between chromosomes as the application of non-destructive defect examination method with fluorescent microscope is such an effective method to obtain the distance of chromosomes that it is expected to actual use in medical diagnosis.

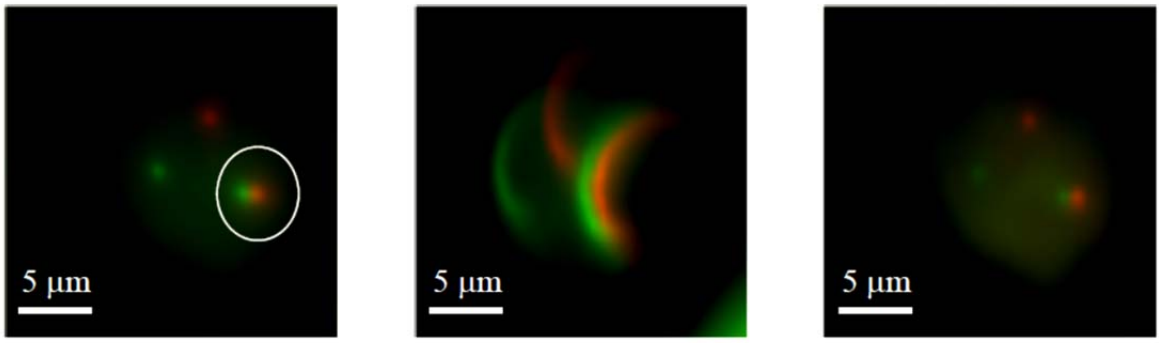


Figure 3-21 Images of stained cell by UtoVysion FISH kit

(a) captured image by the first exposure process
(b) captured image by the second exposure process
(c) captured image when x, y, and z stages were fixed (reference image)

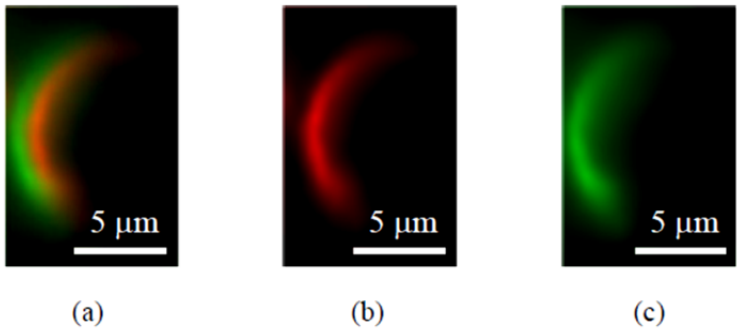


Figure 3-33 Images for calculation of z position

(a) cropped image from figure 3-32
(b) red channel image of figure 3-33(a)
(c) green channel image of figure3-33(a)

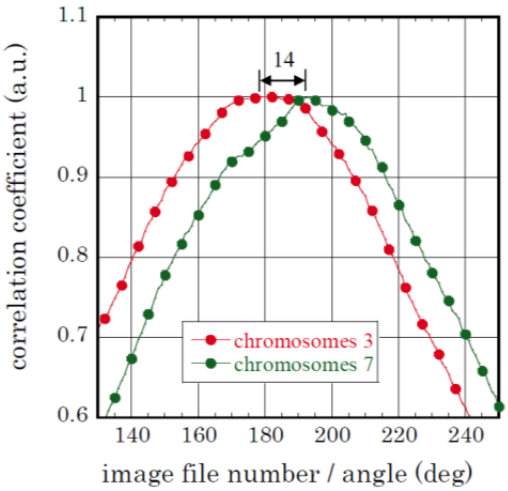


Figure 3-34 Calculation result of z positions

3-8 Summary

In EPIC substrate which consists of silicon layer for CMOS integrated circuits and silicon layer for optical circuits, an impact of defect depends on the layer where the defect exists. Therefore non-destructive defect examination method which pinpoints the layer where defect exists is necessary.

In this chapter, non-destructive defect examination method consists two exposure steps which pinpoints 3D position of defect with 0.1μm and 30nm resolution in air and in silicon, respectively, is proposed and is verified with fluorescent beads placed on the specimen with groove structure. However required data storage size is about 9TB for the defect inspection of one ϕ300mm Si substrate with 20 exposures in depth direction with existing method, the proposed defect examination method which reduces to 1/10 in required data storage size is so effective that it may realize one hundred percent inspection.

Because the cover thickness is changing during exposure in this proposing method, the applicable scanning range is restricted by the existence of spherical aberration. As a method of expanding the scanning range of defect examination, the liquid-crystal panel with ϕ3μm microdots on electrode is proposed and proved that the panel has no diffraction and no beam degradation, and creation of phase profile to compensate the spherical aberration.

As applications of non-destructive defect examination method with fluorescent microscope, measurement of chromatic aberration and measurement of 3D distance of chromosomes in cell are described.

Chapter 4 Fabrication of buried optical waveguide by pattern SIMOX

4-1 Introduction

In this chapter, as a method of keeping with enough quality of surface silicon layer for CMOS electrical circuits, fabricating optical waveguide in second silicon layer from the surface by pattern SIMOX technology proposed in chapter 2 is described.

Experiments are performed with 200mm (8inch) diameter substrate with exception of contamination by using mass production facility of SOI substrates for CMOS electrical circuits. Fundamental processes of SIMOX which are oxygen ion implantation process and high temperature annealing process are performed at Siltronic Japan Corporation at Yamaguchi, Japan where SIMOX SOI substrates are in mass production. Processes of formation of film and pattering of film which are not used in SOI substrate production, are performed at Hitachi Corporation at Tokyo, Japan with a support of Hitachi ULSI Systems Corporation and Hitachi Corporation. An Inspection of contamination is performed every conveying the substrates into clean room at both Siltronic Japan Corporation and Hitachi Corporation in order to check the previous process is suitable for cutting-edge CMOS integrated circuits.

The criterion of defect density on silicon layer for CMOS electrical circuits is set to 1.0 x $10^4/cm^2$ after the fabricating optical waveguide in second silicon layer by pattern SIMOX technology. The defect density of 1.0 x $10^4/cm^2$ is classified to extremely low defect level in ITRS roadmap issued in 2011 corresponds to 22nm node CMOS design rule. The criterion of flatness of surface silicon layer for CMOS electrical circuits is set to 22nm which is regarded as suitable flatness for CMOS electrical circuits.

In section 9, research activities related to buried optical waveguide which is achieved by this research are presented.

4-2 Adoption of mask material for ion implantation

First, mask material for ion implantation in proposing method shown in figure 2-9 is described.

The mask of ion implantation process in this research controls the depth of implanted oxygen, and accelerated oxygen ion penetrates the mask. Therefore in adoption of mask material, knock-in effect [95] is needed to be considered because atoms in mask material are implanted into silicon substrate by collision with ion implanted oxygen by knock-in effect as illustrated in figure 4-1. To prevent contamination of substrate, mask material is preferable to be silicon or silicon dioxide which is composed of substrate materials. Because silicon dioxide which is used in gate material in CMOS transistor has mature processing technology in CMOS fabrication, silicon dioxide made by thermal processing is selected to be mask material.

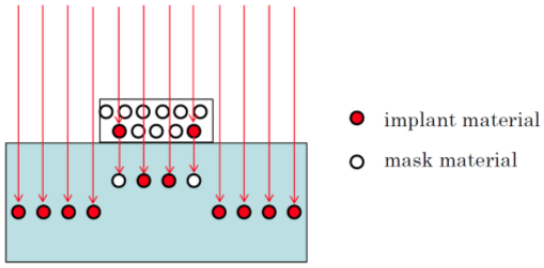


Figure 4-1 Knock-in effect

4-3 Applying device simulator to oxygen ion implantation

In order to perform oxygen ion implantation to SOI substrate and create silicon oxide at implanted position precisely, device simulator is applied. Because temperature of SIMOX annealing process excesses 1300 degree C, 1300 degree C is much higher than annealing temperatures in CMOS fabrication technology.

There isn't enough knowledge on SIMOX annealing process. The device simulator is applied to oxygen ion implantation process in this research.

4-3-1 Adjustment of implantation function to oxygen ion implantation

A semiconductor process simulator which is called as device simulator used at semiconductor manufacturer is suitable for simulating processes for making transistor. There is no command for oxygen ion implantation in device simulator. Existing command of ion implantation is adjusted by measuring the dose profile of oxygen implanted specimen.

Oxygen ion implantation process is ordered to Implant Science (http://implantsciences.com/). As acceleration voltage of ion implantation was limited to 100keV at Implant Science, acceleration voltage is set to 40keV. In case dose of $4.0 \times 10^{17}/cm^2$ at 40keV acceleration voltage causes saturation of oxygen ion density, $1.5 \times 10^{17}/cm^2$ is set to dose. The density profile of implanted oxygen was measured by Secondary Ion Mass Spectrometry (SIMS) at Evans Analytical Group (http://www.eaglabs.com/). Total amount of oxygen atoms within the depth of 0.8μm was only $4.63 \times 10^{16}/cm^2$. The shortage of implanted atoms is considered to lack of reflection effect. A channeling angle which is the incident angle of implanted ions to substrate was 7 degree in both simulation and experiments. The measured implanted oxygen ion density by SIMS is shown in figure 4-2.

In this research, Tsuprem-4, current product name is Athena, which is a device simulator by Silvaco Inc. (http://www.silvaco.com/) is used in adjustment of ion implantation function. Adjustment is performed by fitting between experimental profile and simulated profile of implanted dopants of boron, phosphor, arsenic, and BF_2. As a result, a profile of boron ion implantation at 32keV of acceleration voltage and $4.5 \times 10^{16}/cm^2$ of dose has good fitting in the range from surface to 0.3μm depth where the peak of density profile is. The profile is shown in figure 4-2 as simulation A. In addition, accompanying with pre dose

value of 1.0 x 10^{19}/cm^3 to boron ion implantation at 32keV of acceleration voltage and 4.5 x 10^{16}/cm^2 of dose has good fitting in the range from surface to 0.6μm depth. The profile is also shown in figure 4-2 as simulation B. At the range from surface to 0.02μm depth, it is difficult to fit the measured oxygen profile and simulated ion implantation profile by an existence of natural oxide.

The good fitting condition was also obtained with phosphor ion implantation at 93keV of acceleration voltage. Because obtained condition with boron has closer acceleration voltage with actual experimental acceleration voltage, command with boron is selected to simulate oxygen ion implantation. Therefore at simulation of oxygen ion implantation onto substrate with mask pattern in following section, commands of boron ion implantation with acceleration voltage at 80% of actual voltage is applied.

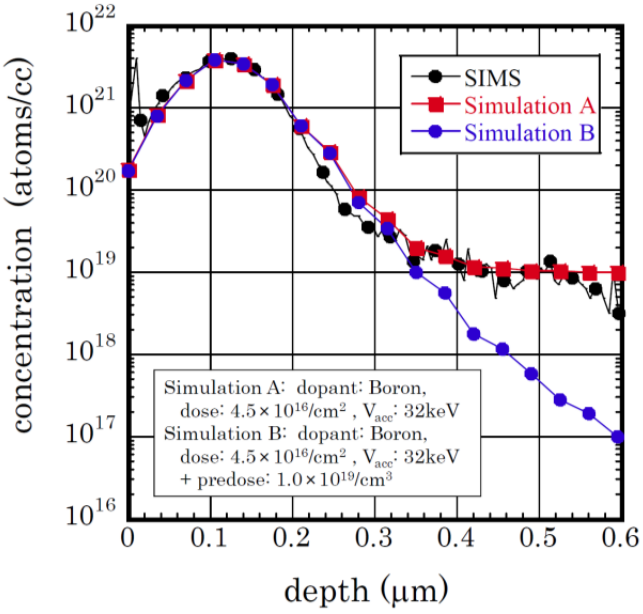


Figure 4-2 Implanted oxygen ion density
SIMS analysis result and simulated profiles

4-3-2 Projection range and dose of implantation onto substrate with mask

Simulated implanted oxygen ion profiles are plotted in figure 4-3. Accelerated voltage is 180keV which is accelerated voltage of 144keV in boron implantation, and dese is 5.0 x $10^{17}/cm^2$. Thickness conditions of mask whose material is silicon dioxide are 50, 100, and 150nm. A channeling angle is 7 degree.

Figure 4-3 shows that the shapes of implanted oxygen density through mask are almost same with shape of implanted oxygen density in case there is no mask. Positions of implanted oxygen density are shifted in the surface direction and shifted distances are almost same with thicknesses of mask.

Two dimensional simulated profile of implanted oxygen ion density into SOI substrate is shown in figure 4-4. The silicon dioxide mask width is 2μm and its thickness is 100nm. SOI thickness is 700nm. Direction of channeling angle of 7 degree is drawn in figure 4-4. From this result, decreasing of projection range is observed in the range with 2.5μm width. The profile of implanted oxygen ion density is asymmetric by the influence of channeling angle.

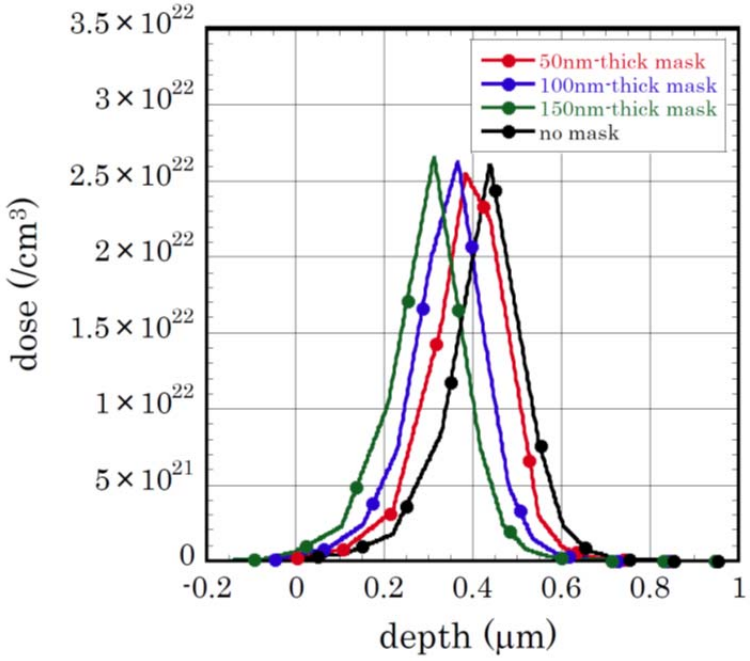


Figure 4-3 Simulated implanted oxygen ion profiles through mask

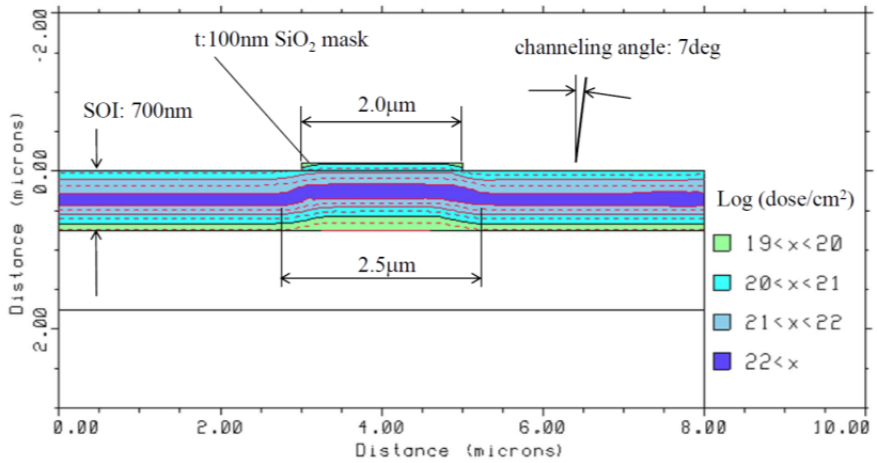


Figure 4-4 2D simulated profile of implanted oxygen ion density into SOI Silicon dioxide mask width and thickness is 2μm and 100nm, respectively

4-4 Specification of SOI substrate

In this section, through simulation of optical properties of buried waveguide made by pattern SIMOX, targeted structure of buried optical waveguide is set and specification of SOI substrate used in this research is described.

4-4-1 Structure of buried optical waveguide

In simulation of optical properties of buried waveguide, FIMMWAVE (Photon Design Ltd. http://www.photond.com/) based on beam propagation method is used. The structure of buried optical waveguide is ridge type waveguide shown in figure 4-5. Beneath the optical waveguide there is 400nm-thick BOX layer made by SmartCut method. Thickness conditions of SOI are 550, 600, 650, and 700nm. The mask used in ion implantation process is made by thermal

oxidation, and its thickness is 50, 100, and 150nm. Because 44% thick silicon is consumed in making silicon dioxide by thermal oxidation process, decreasing of SOI thickness is considered corresponding to mask thickness. From the basic experiment result shown in figure 2-11(a), SIMOX process on SOI substrate made by SOITEC makes 105nm thick silicon dioxide at 170nm depth. At the area where the mask exists, the position of buried oxide is shifted with the thickness of mask. Therefore the rib height of waveguide is same with mask thickness in ion implantation. Although the result of figure 4-4 is not rectangular cross-section, FIMMWAVE only supports rectangular cross-section, so side wall portions of rib waveguide are approximated to rectangular cross-section as shown in figure 4-5.

Simulated radiation loss at the bending position of buried optical waveguide is plotted in figure 4-6. In figure 4-6, horizontal axis is rib height and mask thickness and vertical axis is SOI thickness. At lattice point, the maximum width of rib waveguide which keeps single mode condition is presented in increments of 0.5μm. The radiation loss was calculated at the condition that 1.55μm TE mode guiding light in 1μm width rib waveguide is affected at quarter of a 50μm radius circle. The radiation loss is color-coded in the figure.

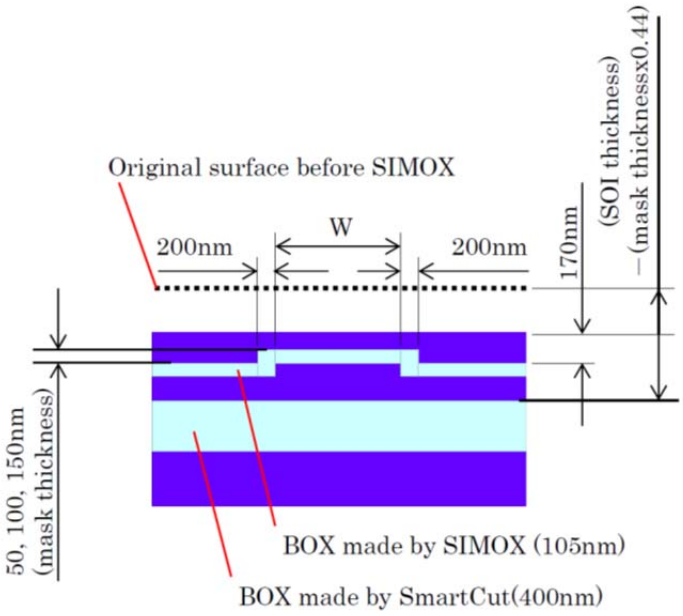


Figure 4-5 Structure of waveguide

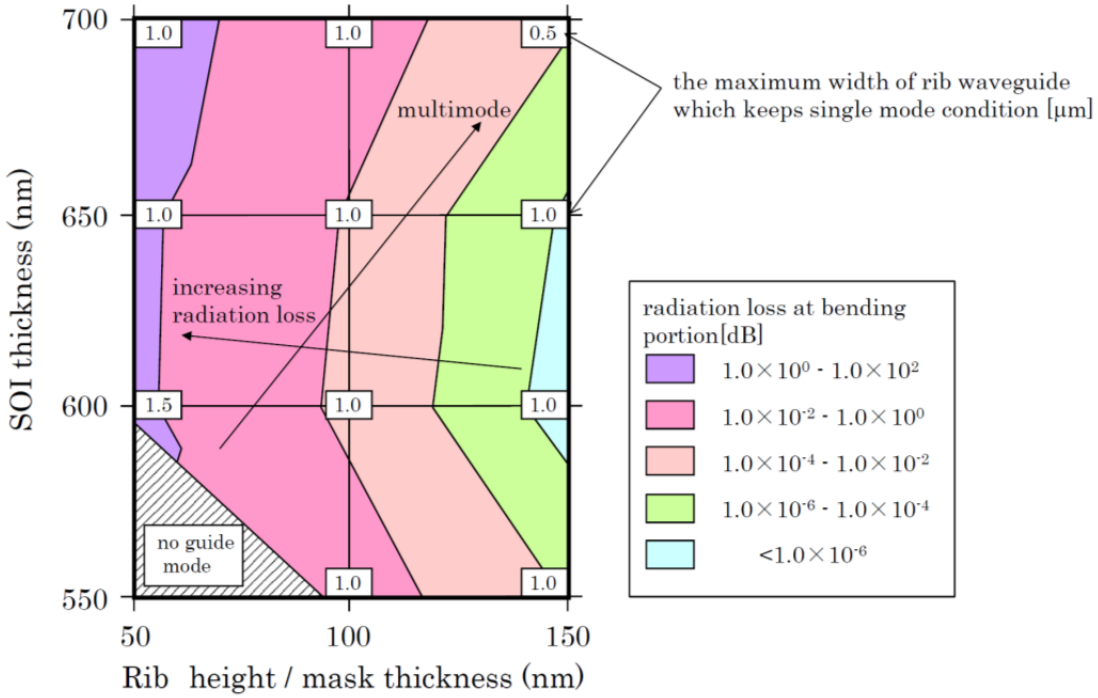


Figure 4-6 Radiation loss at the bending position of buried optical waveguide

Figure 4-6 shows that waveguide condition of thicker SOI and higher rib height has narrower maximum waveguide width for single mode condition. And lower rib height has exponentially larger radiation loss.

The calculated radiation losses at quarter of 25μm, 50μm, and 100μm radius circle are listed in table 4-1. This table indicates increasing radius of bending waveguide decreases radiation loss significantly. The radiation loss at SOI thickness of 650nm, rib height of 100nm, waveguide width of 1μm, and radius of 100μm is negligible value of 1.82 x 10^{-6} dB.

Table 4-1 radiation losses at quarter of 25μm, 50μm, and 100μm radius circle(dB)

	25μm radius			50μm radius			100μm radius		
	rib height(nm)			rib height(nm)			rib height(nm)		
SOI thickness (nm)	50	100	150	50	100	150	50	100	150
550	N/A	1.41×10^{-1}	5.10×10^{-3}	N/A	1.09×10^{-1}	9.78×10^{-5}	N/A	5.11×10^{-2}	6.88×10^{-9}
600	2.46	2.46	1.05×10^{-1}	1.79	4.58×10^{-3}	1.55×10^{-7}	8.29×10^{-1}	2.05×10^{-6}	0
650	3.68	2.54×10^{-1}	4.05×10^{-3}	2.20	7.48×10^{-3}	6.08×10^{-7}	6.41×10^{-1}	1.82×10^{-6}	0
700	5.88	9.58×10^{-1}	6.04×10^{-2}	3.98	1.03×10^{-1}	1.62×10^{-4}	1.70	4.06×10^{-4}	3.78×10^{-10}

From these simulated results, the targeted optical waveguide structure in this research is set to SOI thickness of 650nm and rib height of 100nm. The reason of setting structure is that the radiation loss at waveguide width of 1μm and radius of 100μm is negligible value. In this research, SOI substrate with 650nm thick SOI and 400nm thick BOX is applied because there is no problem in radiation loss simulation and 400nm of BOX thickness is one of standard specifications of SOI substrate made by SOITEC.

4-4-2 Reduction technique of radiation loss at bending waveguide

The buried optical waveguide in this research is located beneath silicon layer for CMOS electrical circuits. In the fabrication process of transistors in CMOS electrical circuits, local oxidation process called LOCOS (Local Oxidation of Silicon) exists to isolate each transistor. Application of LOCOS in reducing radiation loss at bending waveguide is described.

Figure 4-7 shows the basic structure of buried optical waveguide (structure A) that LOCOS reducing radiation loss process has not been applied yet. Figure 4-8 shows the structures of buried optical waveguides (structure B-H) that LOCOS reducing radiation loss process has been applied. The condition of optical waveguides is that rib waveguide with 100nm height and 1μm width is fabricated on 650nm thick and 400nm thick SOI substrate. In order to highlight the efficiency of LOCOS reducing radiation loss, radius of bending waveguide is set to 50μm. As shown in figure 4-7, center of radius is located in the left.

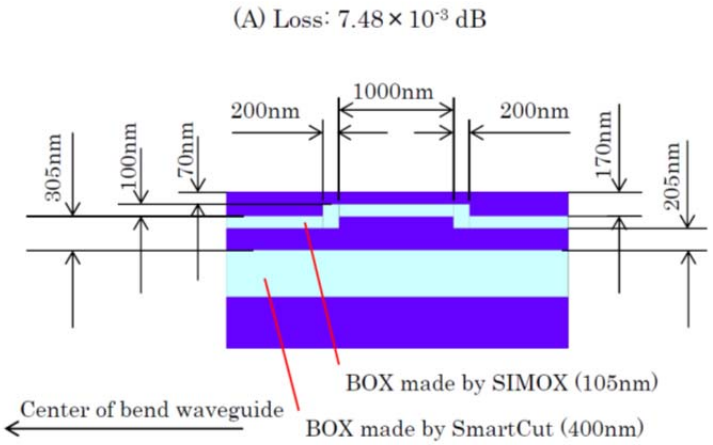


Figure 4-7 Structure of buried optical waveguide (structure A) that LOCOS reducing radiation loss process has not been applied yet

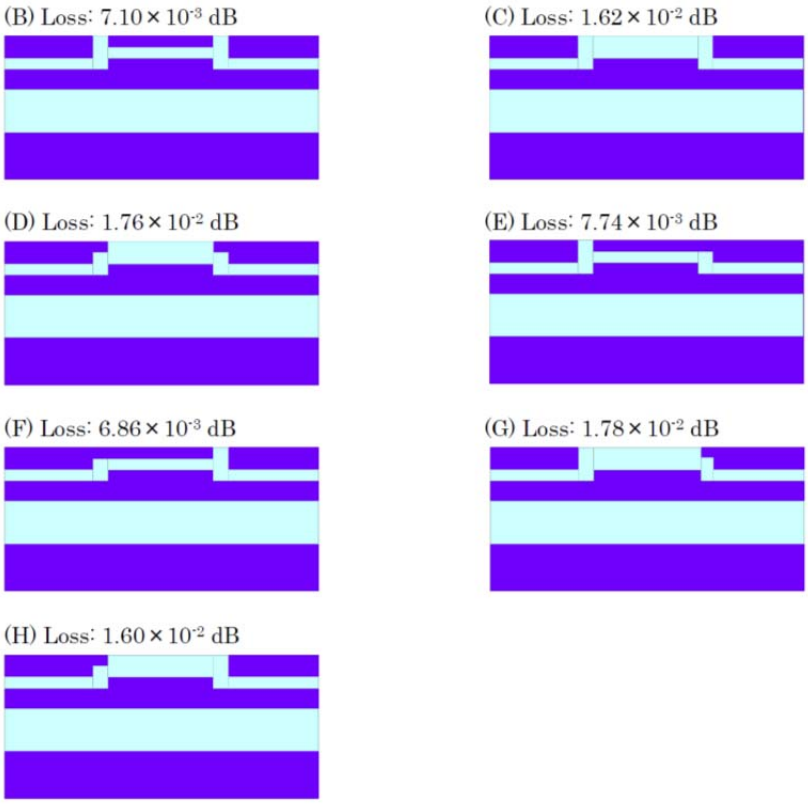


Figure 4-8 Structures and losses of LOCOS reducing radiation technique.

The calculated radiation losses of structures from A to H are plotted at corresponding structure in figures 4-7 and 4-8. Comparing to basic structure shown in figure 4-7, some structures of applied LOCOS reducing radiation

technique shown in figure 4-8 have lower radiation loss. There are slight improvements in structure B and F.

As buried optical waveguide is fabricated in different layer of CMOS circuits in proposing EPIC substrate, proposing EPIC substrate has smaller number of restricted condition than existing EPIC substrate that optical circuits and electrical circuits are located in same silicon layer. So it is easy to apply optical waveguide with bending portion of 100μm radius which has small radiation loss. However proposing EPIC substrate has mild restrictions of applying large radius in bending portion of waveguide, there is reduction technique of radiation loss using LOCOS.

4-4-3 Specification of SOI substrate

The specification of SOI substrate used in this research is shown in table 4-2. Because applying SOI substrate with 400nm thick BOX which is made by SmartCut method at SOITEC, the specification was fixed through discussions with SOITEC considering with high-volume production.

Table 4-2 Specification of SOI substrate

item	parameters	min	target	max	unit
top silicon	SOI thickness	628	650	672	nm
top silicon	crystal orientation	-0.5	<100>	0.5	deg
buried oxide	mean thickness	392.5	400	407.5	nm
handle wafer	crystal orientation	-0.5	<100>	0.5	deg
total	thickness	710	725	740	μm
total	diameter	199.8	200	200.2	mm

4-5 Pattern SIMOX fabrication under standard SIMOX conditions

At first examination of pattern SIMOX fabrication SIMOX, a condition applied to SOI substrate with mask is set to standard SIMOX condition which is used in mass production. The standard SIMOX condition is accelerated voltage of 180keV, dose of 4.0 x $10^{17}/cm^2$, and with ITOX.

4-5-1 Process flow

Process flow of pattern SIMOX fabrication under standard SIMOX condition is shown in figure 4-9.

Formation of silicon dioxide film and mask patterning step was performed at Hitachi Corporation. Silicon dioxide film was formed by thermal oxidation and its thickness was 50nm, 100nm, and 150nm. After patterning of mask on SOI substrate, standard SIMOX process which is oxygen ion implantation and high temperature annealing is performed at Siltronic Japan Corporation. The conditions of standard SIMOX process are accelerated voltage of 180keV, dose of 4.0 x $10^{17}/cm^2$, and annealing at 1350 degree C. After annealing at 1350 degree C standard ITOX annealing was performed. The recipes of high temperature annealing at 1350 degree C and ITOX annealing are confidential.

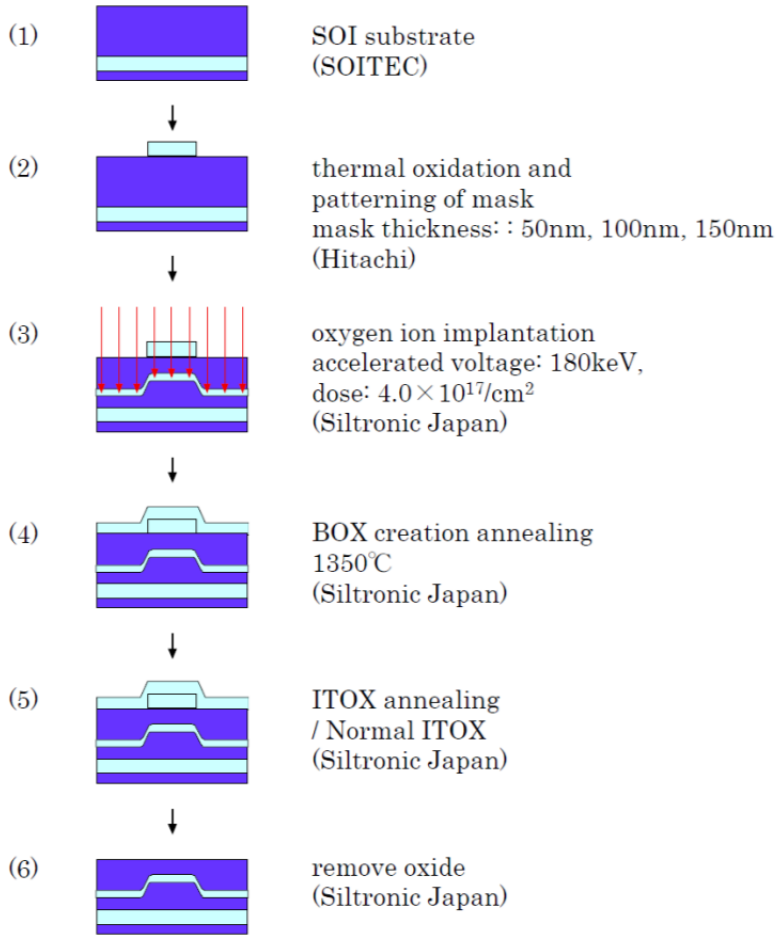
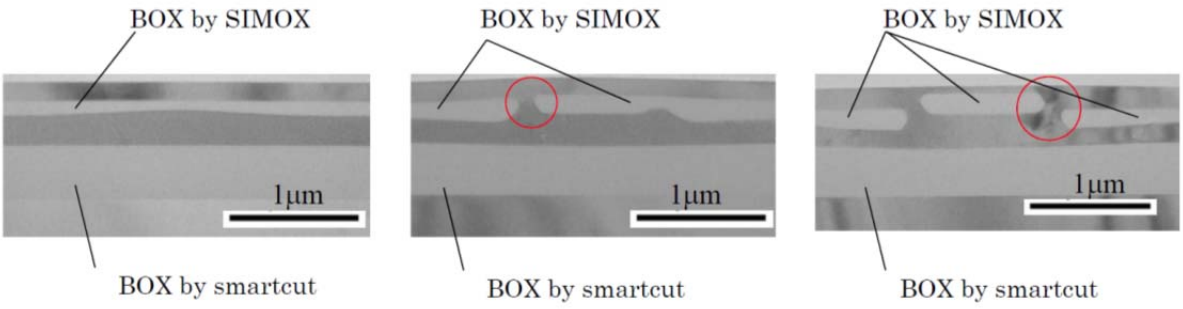


Figure 4-9 Process flow pattern SIMOX fabrication under standard SIMOX

4-5-2 Observation of cross sectional structure

The results of cross sectional observation are shown in figure 4-10. The observation specimen its thickness is from 3 to 5μm is made by Focused Ion Beam (FIB) and these photographs are taken by TEM. All observations in this section are performed where mask width is 1μm.



(a) 50nm thick mask (b) 100nm thick mask (c) 150nm thick mask

Figure 4-10 Cross sectional TEM observation

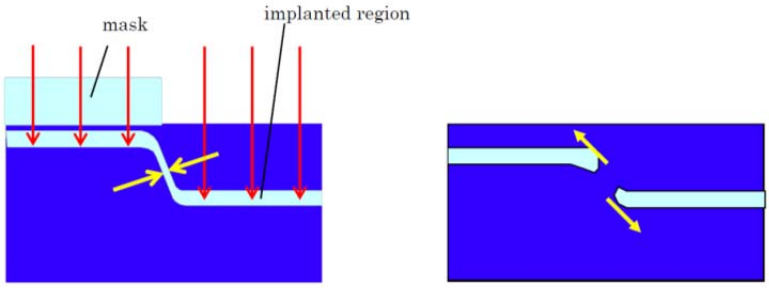
Obtained results from figure 4-10 are written in the followings.

1. As mask thickness increases, depth of BOX layer made by SIMOX under the mask shallows.
2. Although BOX layer made by SIMOX is continuous when mask thickness is 50nm, BOX layer made by SIMOX is discontinuous at the edge of mask when mask thickness is 150nm. In case mask thickness is 100nm, there are both continuous case and discontinuous case for BOX layer made by SIMOX at the edge of mask. The defects at discontinuous positions are marked by red circle in figure 4-10.
3. In all cases of mask conditions, thicknesses of BOX layer made by SIMOX are non-uniform. Especially, case of 100nm mask thickness has large thickness variation. However thickness variation of BOX layer made by SIMOX is smaller in case of 50nm mask thickness, BOX layer under the mask is thinner comparing to other cases.

The first result indicates projection range shallows as the thickness of mask increases. The discussions on the second result about discontinuity of BOX layer made by SIMOX and on the third result about thickness variation of the BOX layer are described in the following sessions.

4-5-3 Discussions about discontinuity of BOX layer and defects

Because the discontinuity of BOX layer made by SIMOX is caused at the edge of mask when mask is thick, assumed mechanism of discontinuity is shown in figure 4-11. The mechanism composes two steps. After ion implantation, the area with enough dose value to create BOX layer becomes narrow in case mask is thick as shown in figure 4-11(a). After high temperature annealing, continuous BOX layer is not created at the narrowed position as same in the case of insufficient dose as shown in figure 4-11(b).

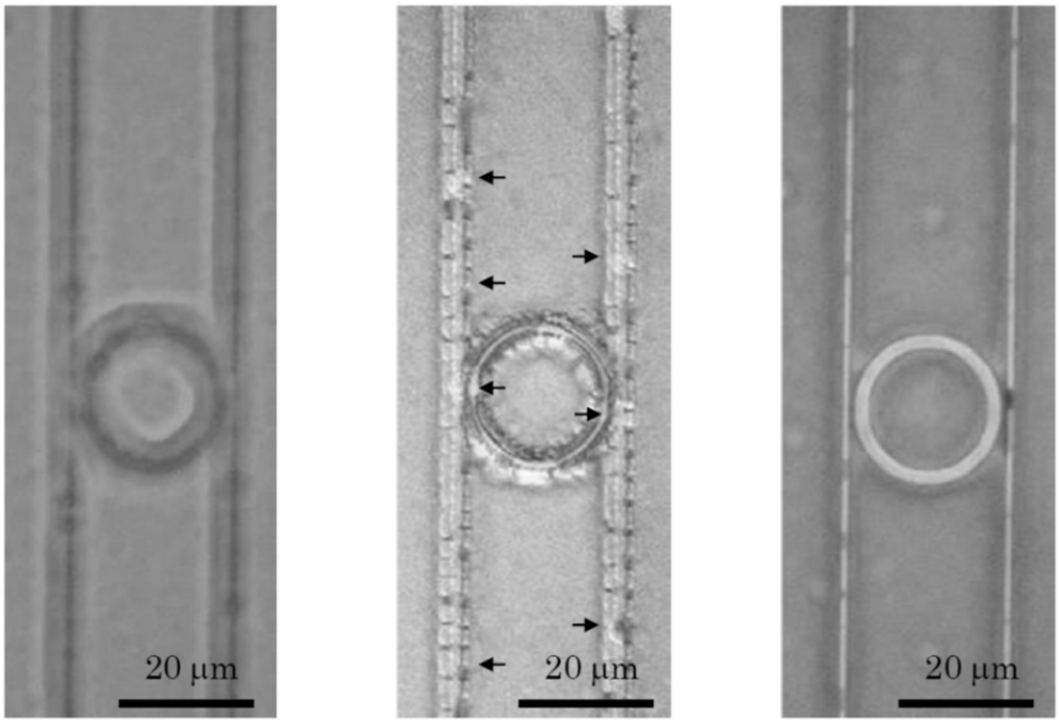


(a) After ion implantation (b) after high temperature annealing

Figure 4-11 Assumed mechanism of discontinuity of BOX layer

From the result that there are defects at highlighted position in TEM photograph of figure 4-10, evaluation of Secco Etching is performed. Figure 4-12 is photographs of silicon surface after Secco Etching taken by optical microscope. When mask is (a) 50nm thick, no defect is observed. When mask is (c) 150nm thick, continuous defect is observed along a mask edge. When mask is (b) 100nm thick, defects are observed at some areas marked with arrows in figure. The locations of defects detected by Secco Etching are indicated to be the discontinuous of BOX layer made by SIMOX as defects are located at the discontinuous of the BOX layer in TEM photograph of figure 4-10. As defects is observed at discontinuous position of BOX layer dominantly even if there is no crack, keeping with continuous BOX layer is required in the aspect of substrate quality.

Because defect is observed along a mask edge, a function of defects ought to be evaluated by unit length. Results of defect evaluation are shown in caption of figure 4-12. In case of (c) mask is 150nm thick, defect density is unable to count because of continuous defect.



(a) (b) (c)

Figure 4-12 Results of defect evaluation (Secco Etching)

(a) 50nm thick mask no defects $<4.7 \times 10^1$/cm
(b) 100nm thick mask defect density 3.3×10^2/cm
(c) 150nm thick mask unable to count defect density

4-5-4 Discussions about thickness variation of BOX layer

The measured thickness of BOX layer made by SIMOX at continuous BOX layer in the specimen whose mask is 100nm thick is plotted in figure 4-13.

The photograph of figure 4-13 shows the cleaved cross section of specimen after 20second treatment of buffered oxide etcher (BOE) which etches silicon

dioxide. At the boundary between silicon and silicon oxide, bright line is observed by electrical charge with SEM observation because silicon has sharp edge.

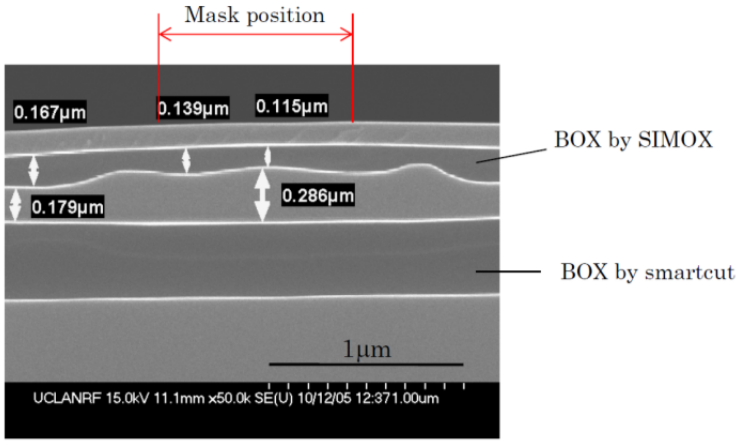


Figure 4-13 Cross sectional observation of 100nm thick mask specimen (SEM)

The expected thickness of BOX layer is 105nm from the SIMOX condition of implanted oxygen and ITOX because simulated implanted oxygen profiles are almost same shown in figure 4-3 except projection range. The thickness of BOX made by SIMOX is thicker than expected thickness, and facilitation of oxidation is observed. Because the position with the maximum BOX thickness of 167nm is not under the mask, the facilitation of oxidation is indicated that it is not from shallow projection range but from non-uniform surface structure at ITOX annealing.

4-5-5 Feedback of experimental results

Because defects are created dominantly where discontinuity of BOX layer made by pattern SIMOX process with transparent mask, it is required to fabricate continuous BOX layer to keep surface silicon layer in enough quality for CMOS electrical circuits. In pattern SIMOX process, ITOX annealing might not grow oxidation uniformly. When the mask exists in ITOX process, the mask might

prevent oxidation under the mask and might cause non-uniform stress around the mask. The mask is indicated to be removed after ion implantation.

4-6 Effect of ITOX annealing at standard dose condition

In this section, derivation of discontinuity of BOX layer in pattern SIMOX process is discussed. In order to make sure that the derivation of discontinuity of BOX layer made by SIMOX is in ion implantation process or in ITOX annealing, experiments with normal ITOX process, slight ITOX, and without ITOX are performed. In addition experiments with adding cover layer on silicon substrates to prevent supply oxygen from ambience are also performed.

From the results of previous section, patterned mask used in ion implantation process is removed before annealing process.

4-6-1 Process flow and its conditions

The process flow of pattern SIMOX in this section is shown in figure 4-14. The removal process of patterned mask after ion implantation is done in Siltronic Japan Corporation. As cover layer to prevent supply oxygen from ambience in annealing 1μm thick silicon dioxide film by low temperature CVD (Low Temperature Oxide: LTO) is applied after removal of patterned mask. The parameters of ITOX annealing are with normal ITOX condition, slight ITOX condition whose facilitation of oxidation is smaller than normal ITOX condition, and without ITOX annealing. The parameters of mask thickness in ion implantation are 100nm, 125nm, and 150nm. The reasons of adding 125nm is to study the phenomena of discontinuity of BOX layer made by SIMOX in detail. The experimental results of cross sectional pictures are shown in appendix 1. In appendix 1, in order to clear effect of mask thickness and ITOX annealing, each

sheet is assembled with the mask width.

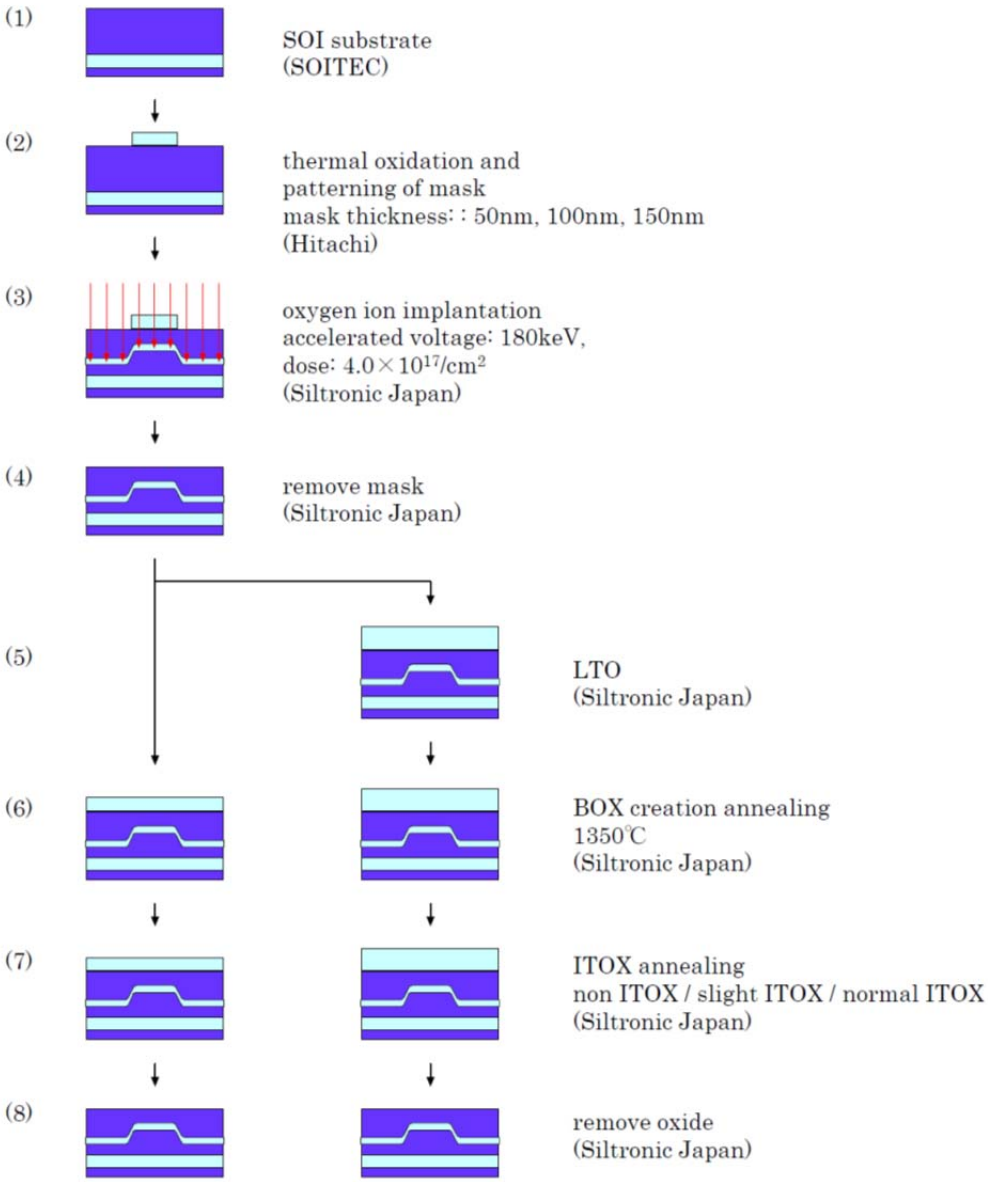
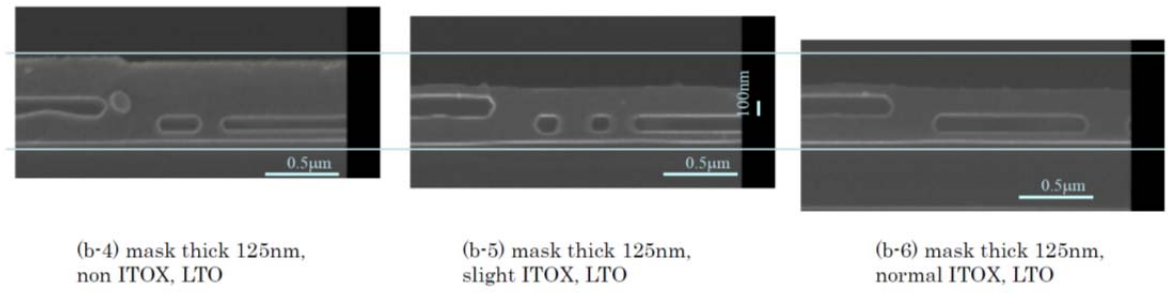


Figure 4-14 Process flow pattern SIMOX fabrication applied with removal of mask and cover layer

4-6-2 Discussion about cover layer (LTO)

In spite of applying LTO as cover layer to prevent supply of oxygen, the cases with LTO and ITOX annealing have thinner SOI than cases without LTO and without ITOX annealing. The representative results are shown in figure 4-15. From these results, LTO is inactive in ITOX annealing process as a cover layer to prevent supply of oxygen. A clear step which was made in ion implantation is observed in case with LTO and without ITOX as shown in figure 4-15(a), LTO is active in BOX creation annealing to prevent supply of oxygen.



(a) without ITOX (b) with slight ITOX (c) with normal ITOX

Figure 4-15 Representative experimental results (case with LTO)
(excerption from figure 1-2 in Appendix)

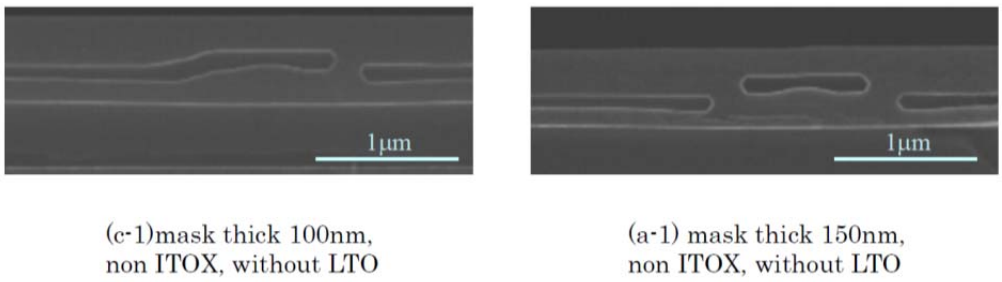
4-6-3 Discussions about discontinuity and thickness variation of BOX layer

In cases without LTO, continuous BOX layer made by SIMOX is created at where there is enough distance from patterned mask. In cases with LTO, continuous BOX layer made by SIMOX is not created at where there is enough distance from patterned mask. From these results, in SIMOX condition of accelerated voltage of 180keV and dose of $4.0 \times 10^{17}/cm^2$, dose is insufficient in cases with LTO. Although discontinuous BOX layer is observed at single side of mask edge in cases with 100nm thick mask as shown in figure 4-16(a), there is no

result with discontinuous BOX at both side of mask edge. In cases with 125nm and 150nm thick mask, there are no results with continuous BOX layer at the mask edge as shown in figure 4-16(b).

In cases without LTO and with ITOX, thicker BOX layer made by SIMOX is observed near discontinuous position. ITOX is not able to connect discontinuous BOX layer after BOX creation annealing, and ITOX enhances the thickness variation of BOX layer near discontinuous position as shown in figure 4-17.

Regarding thickness variation of BOX, thickness variation in this section is smaller than the results in previous section. It is indicated that removal of mask after ion implantation reduces non-uniform oxidation and thickness variation of BOX layer.



(a) 100nm thick mask (b) 150nm thick mask

Figure 4-16 Discontinuity of BOX layer related to mask thickness (excerption from figure 1-2 in Appendix)

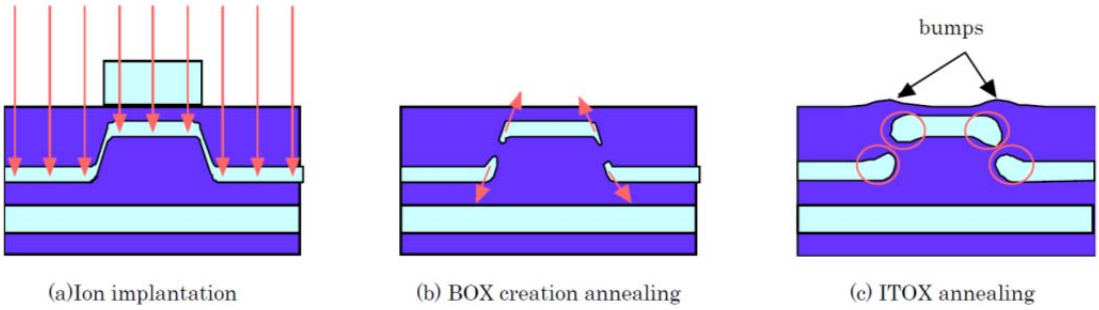


Figure 4-17 Process steps of non-uniform BOX layer near discontinuous position

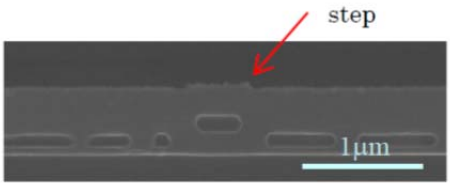
4-6-4 Discussions about step and uneven surface

In cases with LTO and without ITOX, step whose width is same with mask width is clearly observes at the surface as representative result is shown in figure 4-18(a). Because the width of step is same with the width of mask, the step is indicated to be made with sputtering effect at ion implantation process. Figure 4-18(b) is the result of without LTO comparing to the results of with LTO shown in figure 4-18(a). In figure 4-18(b) narrow and smooth uneven surface is observed in case of mask width is (2)2.0μm, but flat surface is observed in case of mask width is (1)0.5μm.

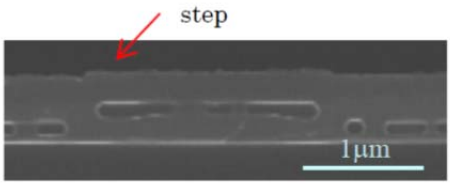
Figure 4-19 shows explanation of consequence of change of steps formed in ion implantation. As same steps were formed in ion implantation, steps shown in figure 4-19(a) change to its shape shown in figure 4-19(b). When mask width is 2.0μm, step is narrowed, and when mask width is 0.5μm, step is disappeared.

Small bumps at edges of mask are observed in case without LTO and with ITOX as shown in figure 4-20. As discussed in figure 4-17, non-uniform oxidation at discontinuous BOX layer at ITOX was occurred. These bumps are indicated to be caused from volume expansion by the non-uniform oxidation at discontinuous BOX layer at ITOX.

From these discussions, there are two origins of uneven surface that are sputtering effect in ion implantation and volume expansion by non-uniform oxidation at discontinuous BOX layer.



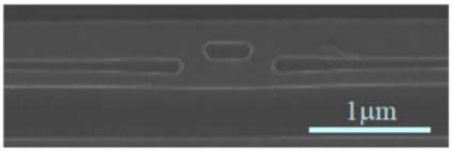
(a-4) mask thick 150nm, non ITOX, LTO, mask width 0.5μm



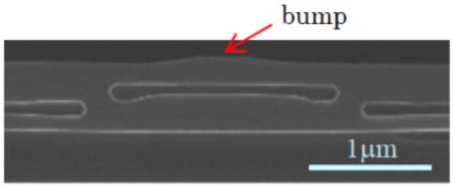
(a-4) mask thick 150nm, non ITOX, LTO, mask width 2.0μm

(1) mask width is 0.5μm (2) mask width is 2.0μm

(a) cases with LTO



(a-1) mask thick 150nm, non ITOX, without LTO, mask width 0.5μm

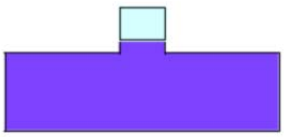


(a-1) mask thick 150nm, non ITOX, without LTO, mask width 2.0μm

(1) mask width is 0.5μm (2) mask width is 2.0μm

(b) cases without LTO

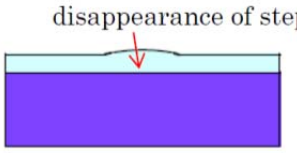
Figure 4-18 Observation of uneven surface comparison of mask width and LTO (excerption from figures 1-2 and 1-4 in Appendix)



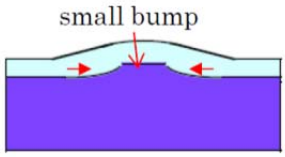
(1) mask width 0.5μm

(2) mask width 2.0μm

(a) after ion implantation



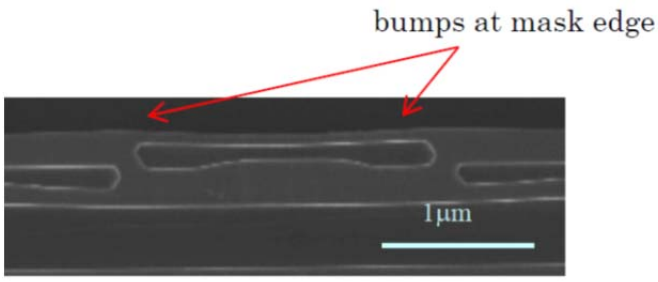
(1) mask width 0.5μm



(2) mask width 2.0μm

(b) after BOX creation annealing

Figure 4-19 Explanation of consequence of change of steps



(a-3) mask thick 150nm, normal ITOX,
without LTO, mask width 2.0μm

Figure 4-20 Bumps caused from volume expansion by the non-uniform oxidation (excerption from figure 1-4 in Appendix)

4-6-5 Discussions about influence on BOX layer made by SmartCut

Influence on BOX layer made by SmartCut is discussed in pattern SIMOX process. Figure 4-21 shows the representative result with mask thickness of 150nm and mask width of 1μm. In this case, the thickness of BOX layer made by SmartCut at under the mask is observed to be 20nm less than other location.

In SIMOX process to bulk silicon substrate, all implanted oxygen is considered to precipitate and form silicon dioxide layer in BOX creation annealing process. But in SIMOX process to SOI substrate, all implanted oxygen is not considered to precipitate and form new silicon dioxide layer in BOX creation annealing process. Some implanted oxygen is indicated to clump existing silicon dioxide layer and grow thickness of existing silicon dioxide layer. In pattern SIMOX process to SOI substrate, implanted oxygen profile is shallow under the mask comparing to around the mask. Implanted oxygen at the location without mask has larger contribution of growing the thickness of existing BOX layer than at the location with mask.

This phenomenon indicates that insufficient dose to create continuous BOX layer is likely to be caused at the location without mask relative to at the location under the mask.

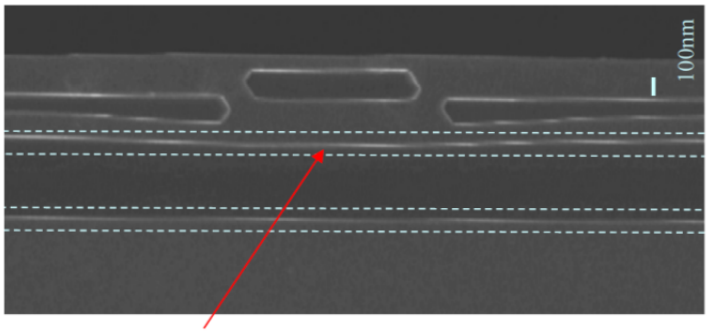
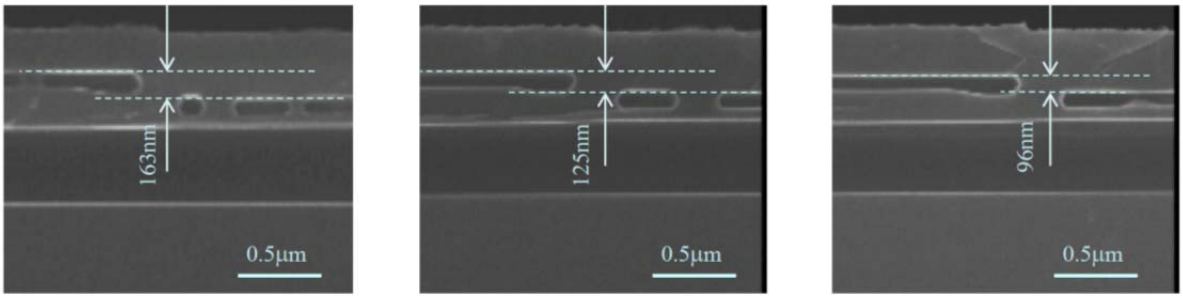


Figure 4-21 Influence on BOX layer made by SmartCut
(excerption from figure 1-2 in Appendix)

4-6-6 Discussions about projection ranges related to mask thickness

The differences of depth position of BOX layer made by SIMOX between under the mask and around the mask are measured. The experimental results used in the measurement are shown in figure 4-22.

Cases without ITOX and with LTO are chosen to minimize the influences of supplied oxygen from ambient. Cases of mask width of 2.0μm are chosen to eliminate the effect of discontinuity of BOX layer and measured at the center position of the mask. The measured depth differences in cases of mask thickness of 100nm, 125nm, and 150nm are 96nm, 125nm, and 163nm, respectively. These results are plotted along with simulation results by Tsuprem4 in figure 4-23. However experimental results have 10% larger differences, there is a good agreement. The target lib height of buried waveguide is expected to be realized when mask thickness is 100nm.



(a-4) mask thick 150nm, non ITOX, LTO, mask width 2.0μm

(b-4) mask thick 125nm, non ITOX, LTO, mask width 2.0μm

(c-4) mask thick 100nm, non ITOX, LTO, mask width 2.0μm

(a) 150nm thick mask (b) 125nm thick mask (c) 100nm thick mask

Figure 4-22 Measured depth difference of BOX layer
(excerption from figure 1-4 in Appendix)

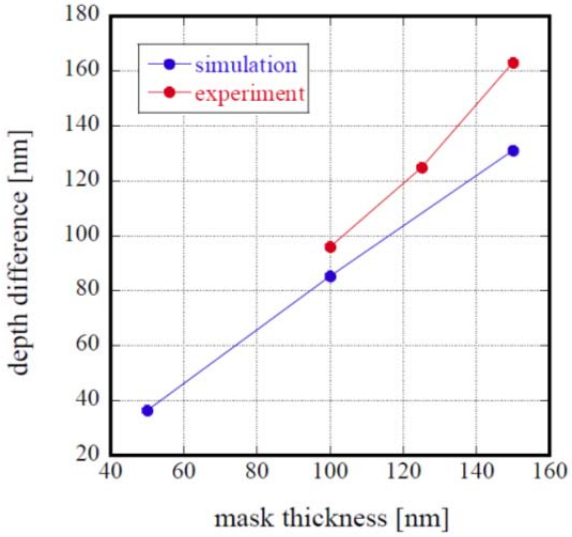


Figure 4-23 Depth difference of BOX layer

4-6-7 Feedback of experimental results

Under the dose condition of 4.0 x $10^{17}/cm^2$, continuous BOX layer at the edges of mask is unable to be created when the mask thickness is 100nm, 125nm, and 150nm. And in cases with LTO, continuous BOX layer made by SIMOX is not created at where there is enough distance from patterned mask. Because thicker BOX layer made by SIMOX is observed near discontinuous position, ITOX is not

able to connect discontinuous BOX layer after BOX creation annealing. Therefore discontinuity of BOX layer at the edges of mask is brought by insufficient dose, so dose value is required to be increased.

Regarding the unevenness at the surface, there are two origins of uneven surface that are sputtering effect in ion implantation and volume expansion by non-uniform oxidation at discontinuous BOX layer. So a prevention of sputtering of surface at ion implantation process is also required. Because in SIMOX process to SOI substrate, all implanted oxygen is not considered to precipitate and form new silicon dioxide layer in BOX creation annealing process, it is indicated that insufficient dose to create continuous BOX layer is likely to be caused relative to SIMOX process to bulk silicon.

As removal of mask after ion implantation reduces non-uniform oxidation and thickness variation of BOX layer, the removal of mask after ion implantation is used in the following sections. Because the target lib height of buried waveguide is turned to be realized when mask thickness is 100nm, mask thickness is fixed to 100nm in the following sections.

4-7 Pattern SIMOX with increasing dose

In this section, pattern SIMOX experiments with dose of 4.5 x $10^{17}/cm^2$, 5.0 x $10^{17}/cm^2$, and 5.5 x $10^{17}/cm^2$ are performed. The formation of continuous BOX layer made by SIMOX at mask edges and at where there is enough distance from patterned mask is remarked.

4-7-1 Process flow and its conditions

Process flow of pattern SIMOX in this section is shown in figure 4-24. The thickness of mask is fixed to 100nm. The parameters of ITOX annealing are also

with normal ITOX condition, slight ITOX condition, and without ITOX annealing. The experimental results of cross sectional pictures are shown in appendix 2. In appendix 2, in order to clear effect of dose and ITOX annealing, each sheet is assembled with the mask width.

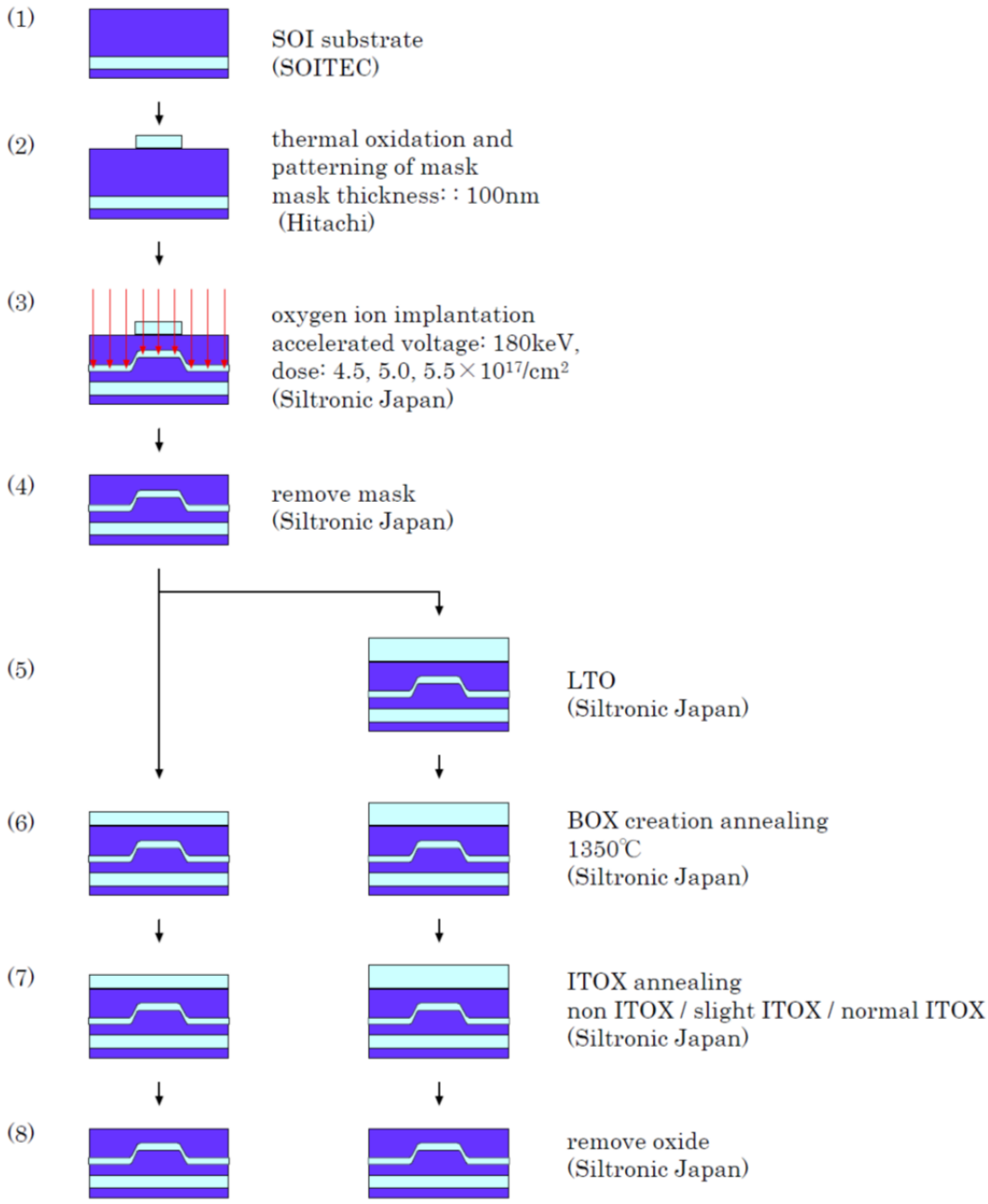
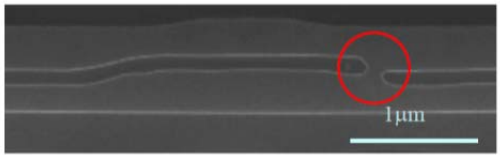


Figure 4-24 Process flow pattern SIMOX fabrication

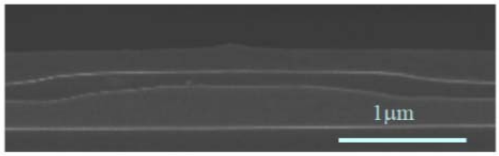
4-7-2 Discussions of continuity of BOX layer

In cases without LTO, however some condition in dose of 4.5 x 10^{17}/cm^2 has discontinuous BOX layer made by SIMOX at edge of mask, conditions in dose of 5.0 x 10^{17}/cm^2 and 5.5 x 10^{17}/cm^2 have continuous BOX layer made by SIMOX at edge of mask. Figure 4-25(a) shows discontinuous BOX layer condition in dose of 4.5 x 10^{17}/cm^2. In figure 4-25(a) position of discontinuous BOX layer is marked with red circle. Figure 4-25(b) and (c) shows representative results of continuous BOX layer condition in dose of 5.0 x 10^{17}/cm^2 and 5.5 x 10^{17}/cm^2, respectively. In all cases, the formation of continuous BOX layer made by SIMOX at where there is enough distance from patterned mask is obtained.



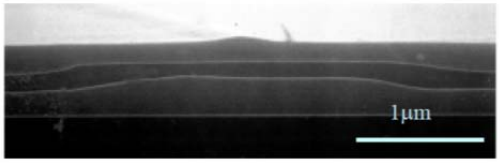
(a-1) 4.5×10^{17}/cm^2, non ITOX,
without LTO, mask width 2.0μm

(a) dose: 4.5 x 10^{17}/cm^2 (excerption from figure 2-4 in Appendix)



(b-3) 5.0×10^{17}/cm^2, normal ITOX,
without LTO, mask width 2.0μm

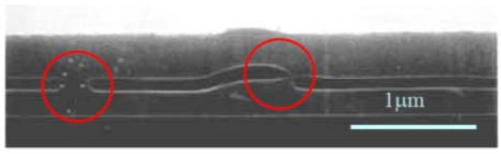
(b) dose: 5.0 x 10^{17}/cm^2 (excerption from figure 2-4 in Appendix)



(c-3) 5.5×10^{17}/cm^2, normal ITOX,
without LTO, mask width 2.0μm

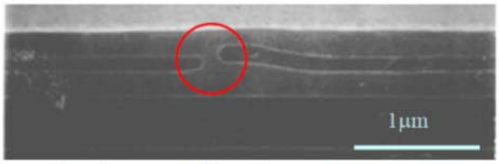
(c) dose: 5.5 x 10^{17}/cm^2 (excerption from figure 2-4 in Appendix)

Figure 4-25 Results in cases without LTO



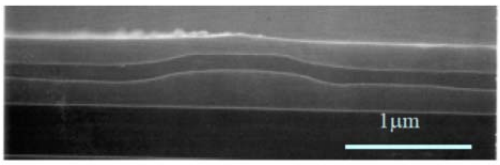
(a-4) $4.5\times10^{17}/cm^2$, non ITOX,
LTO, mask width 0.5μm

(a) dose: 4.5 x $10^{17}/cm^2$ (excerption from figure 2-1 in Appendix)



(b-5) $5.0\times10^{17}/cm^2$, slight ITOX,
LTO, mask width 0.5μm

(b) dose: 5.0 x $10^{17}/cm^2$ (excerption from figure 2-1 in Appendix)



(c-5) $5.5\times10^{17}/cm^2$, slight ITOX,
LTO, mask width 1.0μm

(c) dose: 5.5 x $10^{17}/cm^2$ (excerption from figure 2-2 in Appendix)

Figure 4-26 Results in cases with LTO

In cases with LTO, at condition of dose of 4.5 x $10^{17}/cm^2$, discontinuous BOX layer made by SIMOX is observed at edge of mask and even at where there is enough distance from patterned mask. So in cases with LTO, dose of 4.5 x $10^{17}/cm^2$ is still insufficient. The representative result in condition in dose of 4.5 x $10^{17}/cm^2$ is shown in figure 4-26(a), and positions of discontinuous BOX layer are marked with red circle.

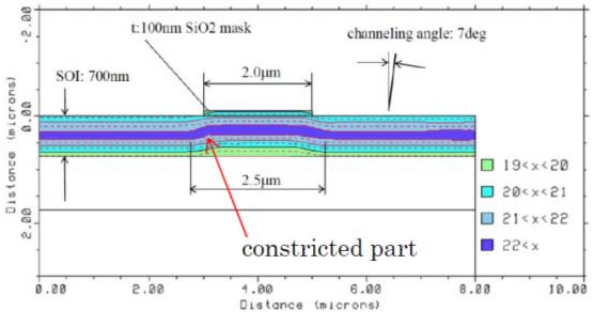
In dose of 5.0 x $10^{17}/cm^2$ and 5.5 x $10^{17}/cm^2$, the formation of continuous BOX layer made by SIMOX at where there is enough distance from patterned mask is obtained. In dose of 5.0 x $10^{17}/cm^2$, discontinuous BOX layer is observed at single side of mask edge, there is no result with discontinuous BOX at both side of mask edge. The representative result in condition in dose of 5.0 x $10^{17}/cm^2$ is

shown in figure 4-26(b), and position of discontinuous BOX layer is marked with red circle. In dose of 5.5 x $10^{17}/cm^2$, continuous BOX layer is observed. The representative result in condition in dose of 5.5 x $10^{17}/cm^2$ is shown in figure 4-26(c).

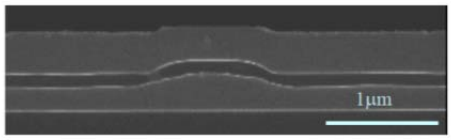
4-7-3 Discussion about asymmetry of BOX layer

In cases of dose of 4.5 x $10^{17}/cm^2$ and in cases with LTO and dose of 5.0 x $10^{17}/cm^2$, discontinuous BOX layers are observed at single side of mask edge. In cases without ITOX annealing, by scrutiny of the condition with continuous BOX layer, asymmetry of BOX layer is observed. The case of asymmetry of continuous BOX layer and simulated result shown in figure 4-4 are shown in figure 4-27. From figure 4-27, both cases have similar asymmetric profiles. The shape of BOX layer in result of case of dose of 5.0 x $10^{17}/cm^2$ has good agreement with density profile of 1.0 x $10^{22}/cm^3$ in simulation. Therefore the asymmetric BOX shape is indicated to be brought from channeling angle in ion implantation.

Based on the assumed mechanism of discontinuity of BOX layer shown in figure 4-11, the location of discontinuity at single side of mask edge is indicated to be at constricted part where is marked with arrow in figure 4-27(a).



(a) simulated dose profile (figure 4-4)



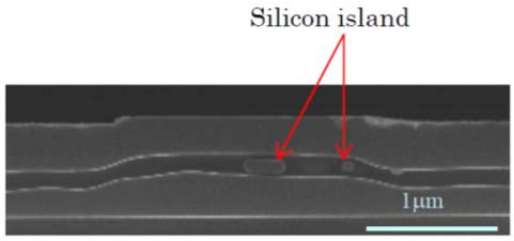
(b-4) $5.0\times10^{17}/cm^2$, non ITOX, LTO, mask width 1.0μm

(b) experimental result dose: 5.0 x $10^{17}/cm^2$ without ITOX (excerption from figure 2-2 in Appendix)

Figure 4-27 Comparison of simulated dose profile and BOX shape

4-7-4 Discussion about silicon island

Some results in dose of 5.5 x $10^{17}/cm^2$ have silicon island which is the phenomenon of residual silicon portion in BOX layer made by SIMOX. The representative result having silicon island is shown in figure 4-28. Because in the structure of silicon island, island shape silicon which is conductive material with index of 3.5 exists in dielectric material of silicon dioxide with index of 1.5, isolation performance of silicon dioxide is degraded in electrical property and propagation loss is increased brought by deviation of clad index in optical property. As silicon island is reported to appear with excess dose conditions [47], dose of 5.5 x $10^{17}/cm^2$ is indicated to be over value when accelerated voltage is 180keV.



(c-4) $5.5 \times 10^{17}/cm^2$, non ITOX,
LTO, mask width 2.0μm

Figure 4-28 Silicon island (dose: 5.5 x $10^{17}/cm^2$)
(excerption from figure 2-4 in Appendix)

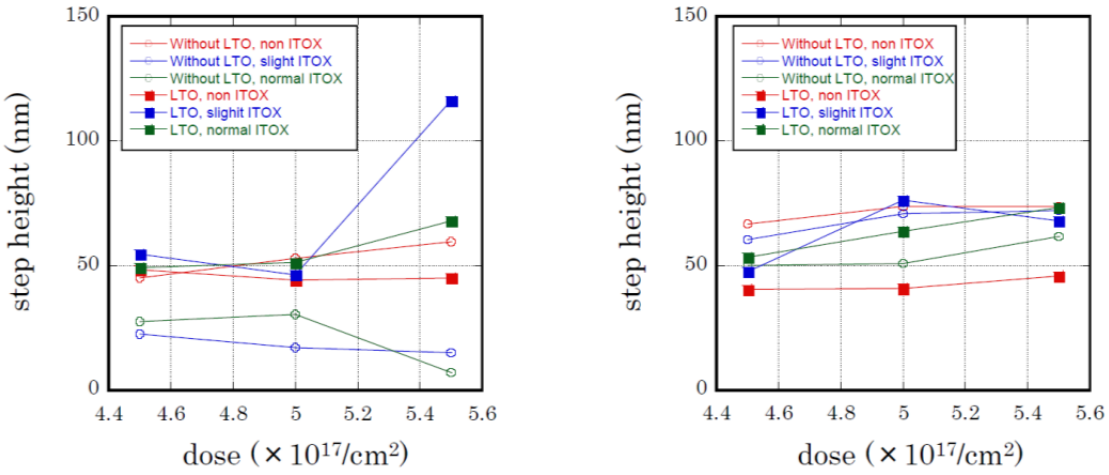
4-7-5 Discussion about surface flatness

The surface profiles of specimens with mask width of 1μm and 2μm are measured with atomic force microscope (AFM) by Veeco Instruments, Inc. (http://www.veeco.com/). The measured maximum height is plotted in figure 4-29. The measured length is 50μm including mask portion. From the results of mask width of 1μm, the maximum height of surface is decreased with ITOX annealing in cases without LTO. In cases with LTO, step remains with ITOX annealing.

From the results of mask width of 2μm, the maximum height of surface

increases slightly with dose. As previously presented in figure 4-19, the step created by sputtering in ion implantation remains after annealing when the mask width is 2μm, the step height corresponds to dose.

From the hearing to semiconductor manufacturer, the ideal maximum height is less than 20nm. The step creation at ion implantation with sputtering is requested to be prevented.



(a) mask width: 1μm (b) mask width: 2μm

Figure 4-29 Measured maximum height including mask position by AFM

The measured surface profiles where there is no mask by two-dimensional AFM is shown in figure 4-30. The measurement is performed the specimen with dose of 5.0 x 10^{17}/cm^2. The measured area was 50μm square. From these results, cases with LTO have worse surface profiles and adding ITOX degrade the surface profile further.

In order to compare the surface degradation between mask position and around mask, two-dimensional AFM measurement is performed. Figure 4-31 shows measurement results in cases with LTO and without LTO. From the result of case without LTO (a), the surface around the mask is extremely smooth. But from the result of case with LTO (b), roughness of about 50nm appears on surface regardless of mask position.

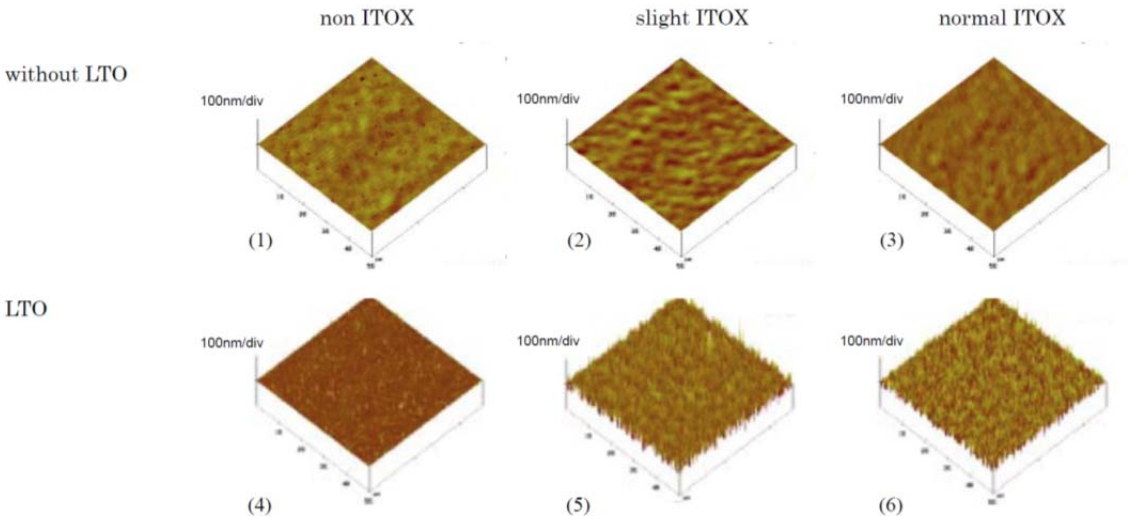
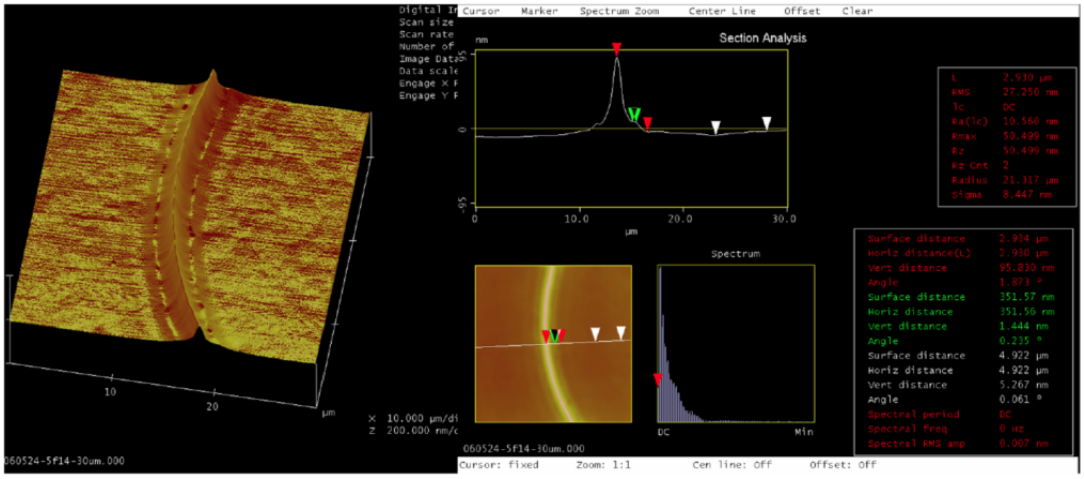
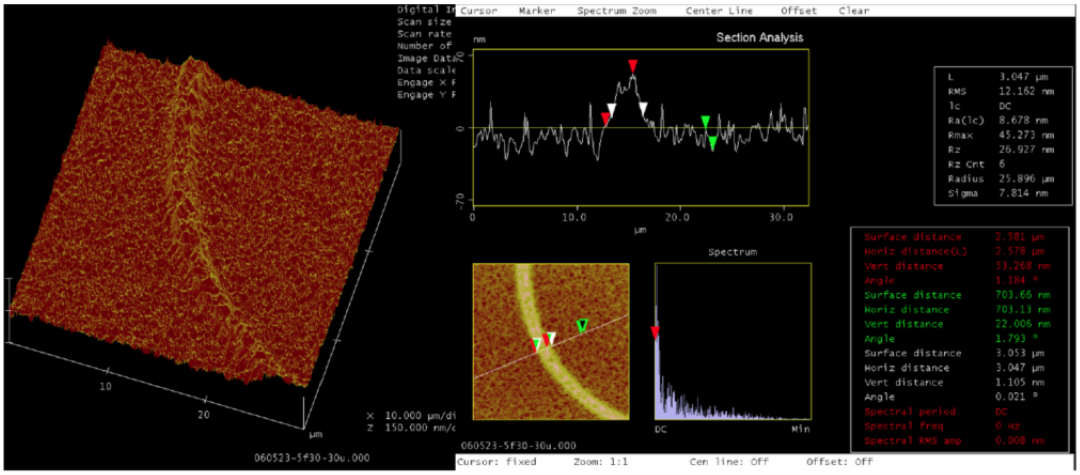


Figure 4-30 Surface profile measured by AFM no mask area



(a) without LTO and with ITOX (dose: 5.0 x 10^{17}/cm^2)



(b) with LTO and with ITOX (dose: 5.0 x 10^{17}/cm^2)

Figure 4-31 Two-dimensional AFM measurement around mask

The cross sectional observation with TEM is examined to analyze surface roughness. Figure 4-32 and 4-33 shows the results of cases with LTO and without LTO, respectively. Specimen condition of both specimens is dose of 5.0 x 10^{17}/cm^2 and without ITOX. From figure 4-32, many defects are observed. From its shape, the defects are considered to be the stacking fault dislocation [96] whose characteristic is half noon shape. On the other hand, there is no defect observed on the surface of case without LTO.

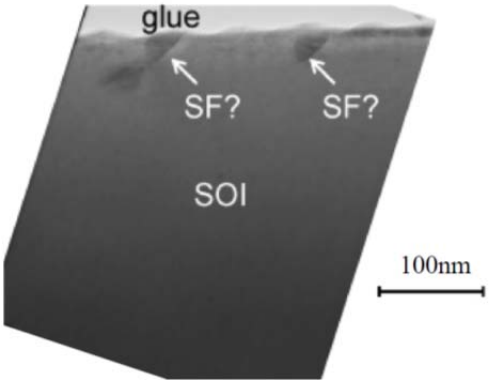


Figure 4-32 Cross-sectional TEM without LTO and with ITOX

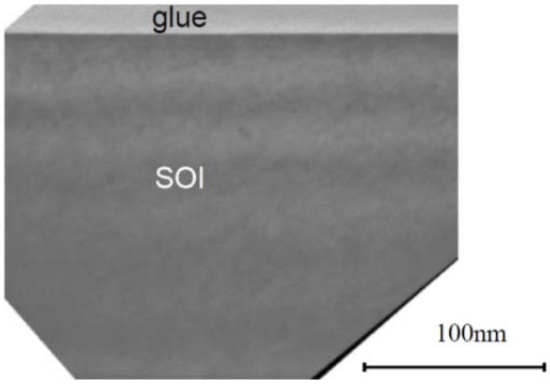


Figure 4-33 Cross-sectional TEM with LTO and with ITOX

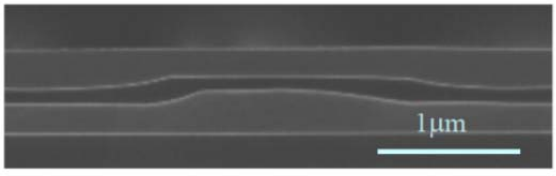
4-7-6 Feedback of experimental results

In this section, pattern SIMOX experiments with dose of 4.5 x 10^{17}/cm^2, 5.0 x 10^{17}/cm^2, and 5.5 x 10^{17}/cm^2 are performed. Dose is increased to realize continuous BOX layer. To obtain continuous BOX layer and suppression of silicon island in BOX layer, following two SIMOX conditions exist.

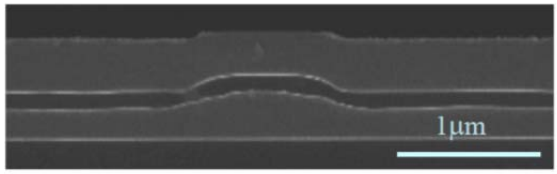
(candidate A) dose of 4.5 x 10^{17}/cm^2, with ITOX, and without LTO

(candidate B) dose of 5.0 x 10^{17}/cm^2, without ITOX, and with LTO

The obtained results at these conditions in this section are shown in figure 4-34. The mask width of these results is 1μm.



(a-3) $4.5\times10^{17}/cm^2$, normal ITOX, without LTO, mask width 1.0μm



(b-4) $5.0\times10^{17}/cm^2$, non ITOX, LTO, mask width 1.0μm

(a) candidate A (b)candidate B

Figure 4-34 Cross sectional structure of candidate conditions

The width of waveguide structure of candidate A is widened comparing to candidate B. This structure has a disadvantage in increasing the density of optical circuits. On the other hand, the waveguide structure of candidate B has good agreement with simulated profile of dose density at ion implantation. Therefore width of waveguide structure of candidate B is not widened, and waveguide structure obtained with this condition is easy to simulate.

From increasing the optical circuit density point of view, the waveguide structure of candidate B is preferable.

In next section, process optimization is performed on the pattern SIMOX process of candidate B.

Process optimizations are required in three points.

1. reduction of asymmetry of BOX layer made by SIMOX
2. prevention of surface defects by remediation of material
3. prevention of step formation by sputtering in ion implantation

4-8 Optimization of pattern SIMOX

In this section, process optimization is performed on the pattern SIMOX process of candidate B which is dose of 5.0 x $10^{17}/cm^2$, without ITOX, and with LTO. The obtained waveguide structure made by pattern SIMOX with

optimizations is presented.

4-8-1 Reduction of asymmetry of BOX layer made by SIMOX

In order to reduce the asymmetry of BOX layer made by SIMOX, an SOI substrate is rotated with 90 degree every dose of 1.25 x $10^{17}/cm^2$ which is quarter of total dose of 5.0 x $10^{17}/cm^2$. Figure 4-35 shows the conceptual profile of oxygen density with dose of 5.0 x $10^{17}/cm^2$ at ion implantation, in this picture channeling angle is rotated with 90 degree every dose of 1.25 x $10^{17}/cm^2$. The areas with enough distance from mask and under the center of mask have stable dose density regardless the substrate rotation. But around the edge of mask, the concentration of density of implanted oxygen is diffused. From simulated results of implanted density shown in figure 4-4, the value of asymmetry is about 50nm. Because asymmetry value of 50nm is more than one digit smaller than mask width of 1μm, diffusion of ion implantation density at the edge of mask is regarded to be negligible.

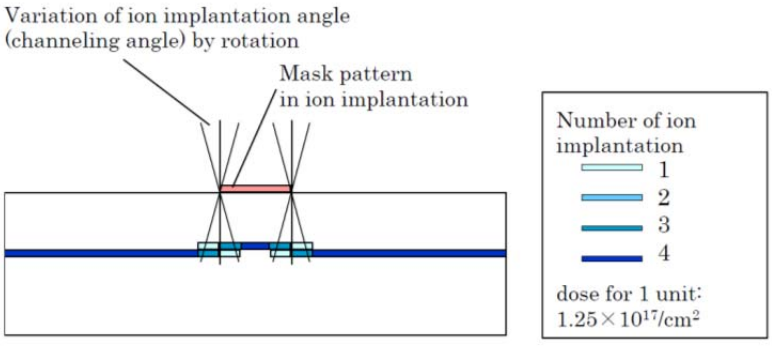


Figure 4-35 Conceptual profile of oxygen density with 90 degree rotation every quarter dose of total dose.

4-8-2 Prevention of surface defects by remediation of material

As observed defects at the surface of case with LTO are brought from adding LTO as a protective layer of supply oxygen in annealing, materials of film layer to protect supply oxygen are investigated. The investigated materials are chosen from the adaptable material list of CMOS fabrication process at Hitachi Corporation at Tokyo. Because annealing temperature at 1350 degree C of BOX creation annealing process excesses usual annealing temperature in CMOS fabrication, there is no knowledge in CMOS fabrication manufactures.

The list of investigated materials is shown in table 4-3. The evaluation points are blocking property of oxidation at 1350 degree C annealing and prevention property of defects formation through BOX creation annealing and normal ITOX annealing. Methods of evaluation are written in followings.

(1) Evaluation of blocking property of oxidation

SOI substrate with 350nm thick of SOI is applied. After forming the candidate film, BOX creation annealing at 1350 degree C is performed. The thickness of SOI layer is optically measured after removal of film. If the measured thickness of SOI is 350nm, blocking property of oxidation is perfect. As a reference, SOI without film is also evaluated.

(2) Evaluation of prevention property of defects formation

SOI substrate with 350nm thick of SOI is also applied. After forming the candidate film, BOX creation annealing at 1350 degree C is performed. And SOI substrates after BOX creation annealing are cleaved and half of SOI substrates are performed with following normal ITOX annealing. Surface inspection with AFM is performed to SOI substrate after BOX creation annealing and SOI substrate after BOX creation annealing and following normal ITOX annealing. The evaluation function is surface roughness and area of AFM inspection is 50μm square.

Table 4-3 List of investigated materials

name	composition	method	thickness(nm)	deposition temperature(℃)	remarks
NSG	SiO2	normal pressure CVD	465	500	NSG : Non doped Silicate Glass
HDP	SiO2	High Density Plasma CVD	370	700	
CVD-SiO	SiO2	reduced pressure CVD	500	800	
CVD-SiO	SiO2	reduced pressure CVD	200	700	
LP-SiN	SiN	reduced pressure CVD	140	800	10nm thick SiO_2 layer required as base coat

Table 4-4 Results of evaluation

film				prevention of oxidation		surface roughness		
name	composition	thickness(nm)	deposition temperature(℃)	SOI(nm)	result	RMS(nm) 1350℃	RMS(nm) 1350℃+ITOX	result
NSG	SiO2	465	500	340	○	0.96	1.15	△
HDP	SiO2	370	700	340	○	0.72	0.99	○
CVD-SiO	SiO2	500	800	345	○	1.16	1.04	○
CVD-SiO	SiO2	200	700	325	×	0.48	0.81	○
LP-SiN	SiN	140	800	350	○	1.96	1.88	×
non coat				310		0.57	0.96	

The evaluation results are shown in table 4-4. The SOI thickness of CVD-SiO film with 200nm is decreased after BOX creation annealing at 1350 degree C, so this film has not blocking property of oxidation. Regarding the prevention property of defects formation, all results have smaller surface roughness than LTO. Because the result of LP-SiN film has double value of reference result of 0.96nm, LP-SiN film is not regarded as available. As the result of NSG film has slightly larger value than reference, NSG film is not regarded as suitable.

From two evaluation results, HDP with 500nm thick and CVD-SiO film with 500nm thick are regarded as adaptable. Among them, HDP with 500nm is applied in pattern SIMOX process because influence of film formation is regarded as small by its lower process temperature.

4-8-3 Prevention of step formation by sputtering in ion implantation

The step height formed at ion implantation with sputtering phenomenon is about 20nm. As a process optimization procedure, additional protecting film is

formed in order to prevent step formation by sputtering. A schematic picture of additional protecting film is shown in figure 4-36. The film 40nm thick of CVD-SiO is applied in experiments.

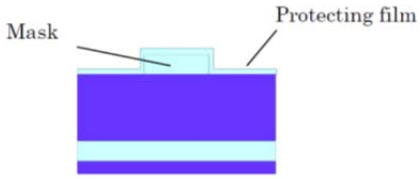


Figure 4-36 Schematic picture of additional protecting film

4-8-4 Fabrication of buried waveguide by optimized pattern SIMOX

The process flow of optimized pattern SIMOX is shown in figure 4-37. ITOX annealing after BOX creation annealing is not applied.

The cross sectional structure is shown in figure 4-38.

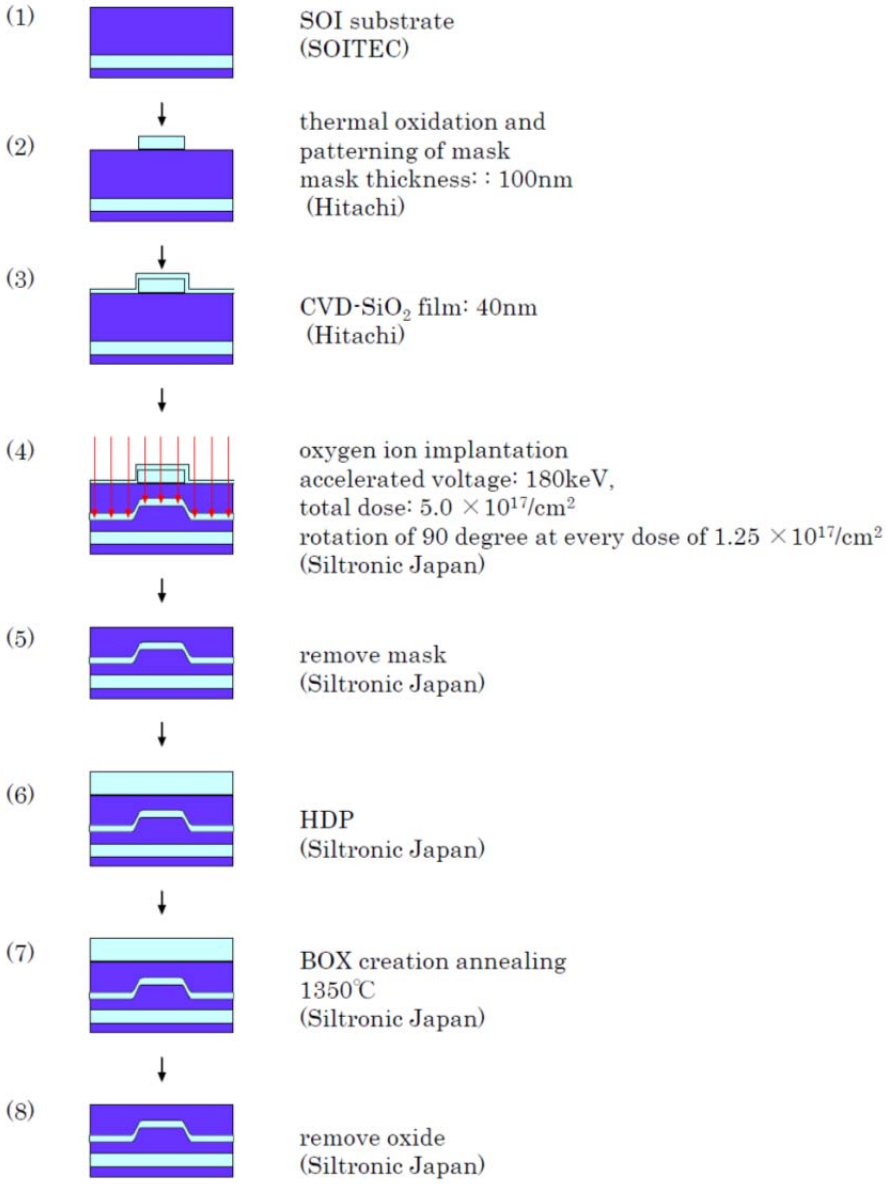
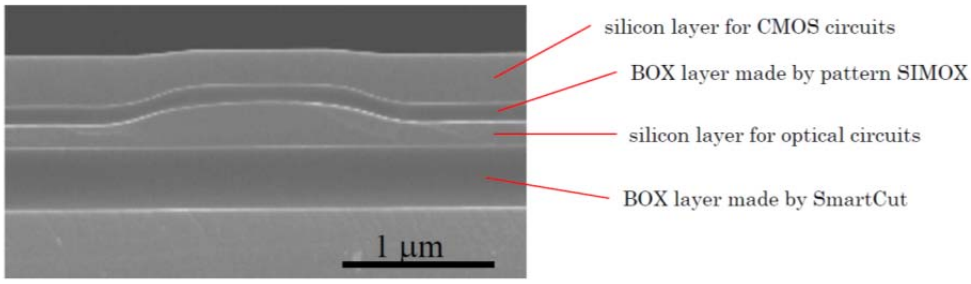
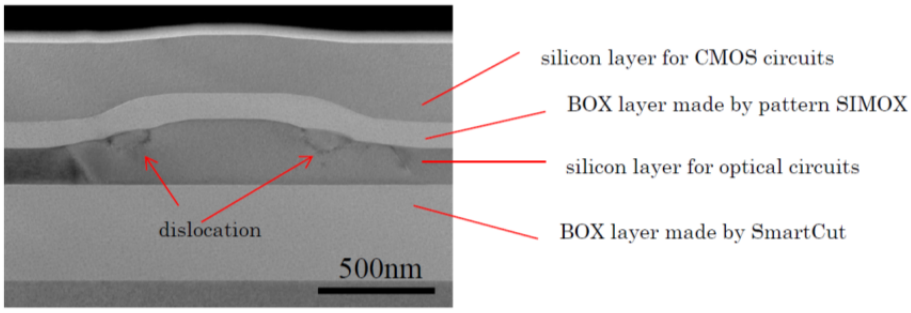


Figure 4-37 Process flow of optimized pattern SIMOX



(a) cross sectional structure with SEM



(b) cross sectional structure with TEM

Figure 4-38 Cross sectional structure obtained by optimized pattern SIMOX

The mask width of the specimen shown in figure 4-38(a) is 1μm. The photograph of figure 4-38(a) is taken with SEM after cleaving of specimen and following BOE etching. The mask width of the specimen shown in figure 4-38(b) is 0.5μm. The photograph of figure 4-38(b) is taken with cross sectional TEM.

From TEM photograph shown in figure 4-38(b), there are no defects in surface silicon layer for CMOS electrical circuits. The measured defect density with Secco Etching was 7.5 x 10^2/cm^2. As the defect density of 1.0 x 10^4/cm^2 is classified to extremely low defect level in ITRS roadmap issued in 2011 corresponds to 22nm node CMOS design rule, the result of defect density at 7.5 x 10^2/cm^2 indicates adequate silicon quality for CMOS electrical circuits is obtained.

Regarding the asymmetry of BOX layer made by pattern SIMOX, symmetrical structure of buried optical waveguide is successively obtained. Even in the condition of mask width of 0.5μm, ridge type optical waveguide is clearly

obtained. Although there are defects in second silicon layer from the surface as a slicon layer for optical circuits, there are no defects in surface silicon layer for CMOS electrical circuits.

The quality of silicon crystal for optical circuits is discussed in the followings. The relation between fabrication process and propagation loss of optical waveguide fabricated on SOI substrate made by high dose SIMOX with 1.8 - 2.0 x $10^{18}/cm^2$ is discussed by Zinke, Ang, and Reed [97-99]. The defect density of SOI substrate made by high dose SIMOX with dose of 2.0 x $10^{18}/cm^2$ is in the range from 2 x $10^8/cm^2$ to 1 x $10^9/cm^2$ [100], and propagation loss of optical waveguide with wavelength of 1.532μm light was reported 0.14dB/cm [99]. It was reported that the propagation loss of waveguide on high dose SIMOX SOI, BE-SOI, and ZMR-SOI (Zone Melting Recrystallized Silicon on Insulator), and SmartCut SOI are almost same [97-99].

TEM cross sectional photograph of high dose SIMOX with dose of 1.6 x $10^{18}/cm^2$ whose defect density is 1 x $10^9/cm^2$ is shown in figure 4-39 [101]. Reed reported that defect in silicon layer does not affect propagation loss unless the defects changes shape of silicon – silicon oxide boundary with using high dose SIMOX substrate [102].

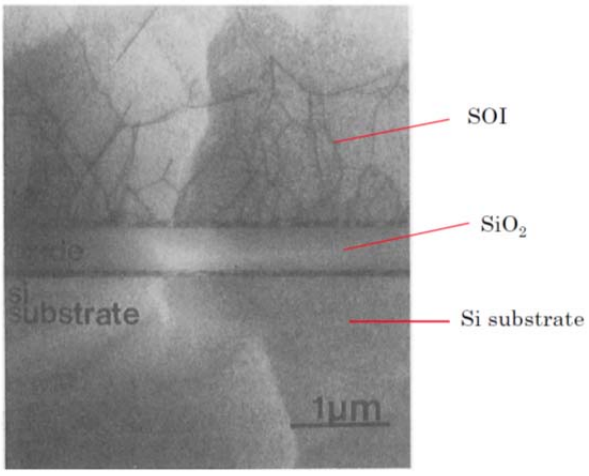


Figure 4-39 Cross sectional TEM photograph of SOI substrate made by high dose SIMOX [101]

Comparing to TEM photographs of figure 4-39 and figure 4-38 which is experimental result of EPIC substrate made by SIMOX of 5.0 x $10^{17}/cm^2$ dose, silicon layer for optical circuits in this paper has uniform contrast and fewer defects, therefore the EPIC substrate obtained in this research has better quality than SOI substrate shown in figure 4-39. It is concluded that silicon layer for optical circuits in this research has enough quality for optical propagation.

Regarding the surface unevenness of EPIC substrate, however 35nm height bump exists at mask position, this bump is very smooth. The comment of semiconductor manufacture is "because this bump is very smooth, it is not considered as 20nm height step which is not suitable for CMOS electric circuits". In addition, the area except for mask position is flat. It is concluded that the surface of EPIC substrate is enough suitable for CMOS circuits.

4-9 Application of buried optical waveguide made by pattern SIMOX

In this section, several cases of application of buried optical waveguide made by pattern SIMOX and expected cases of application are described.

4-9-1 Low propagation loss optical waveguide

As described above, the process of buried optical waveguide with pattern SIMOX has BOX creation annealing at temperature of 1350 degree C. Because this temperature is higher than normal semiconductor process, the boundary between silicon and silicon dioxide is expected to be very smooth comparing to etched surface.

Figure 4-40 shows propagation loss of rib type optical waveguide on SOI substrate by Zinke [97] and buried optical waveguide with pattern SIMOX process

by author in 2003. The pattern of buried waveguide was made with silicon dioxide mask fabricated with manual type contact aligner at University California at Los Angeles. Although in 2011 smaller propagation loss is reported by using stepper which is a manufacturing equipment of semiconductor in mass production [18], figure 4-40 is the comparison of propagation loss of optical waveguides fabricated with contact aligner. From figure 4-40, buried optical waveguide with pattern SIMOX process realized very small propagation loss. This result indicate that the boundary between silicon and silicon dioxide made by SIMOX process is so smooth that pattern SIMOX process is suitable for optical waveguide.

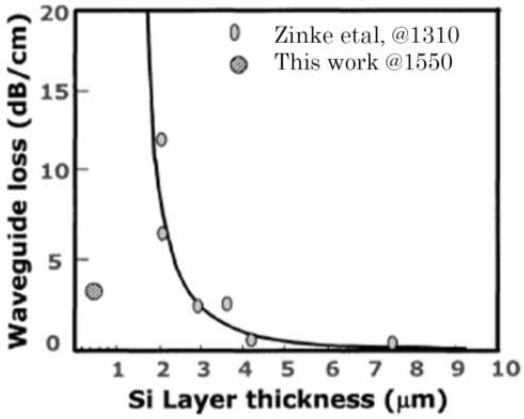


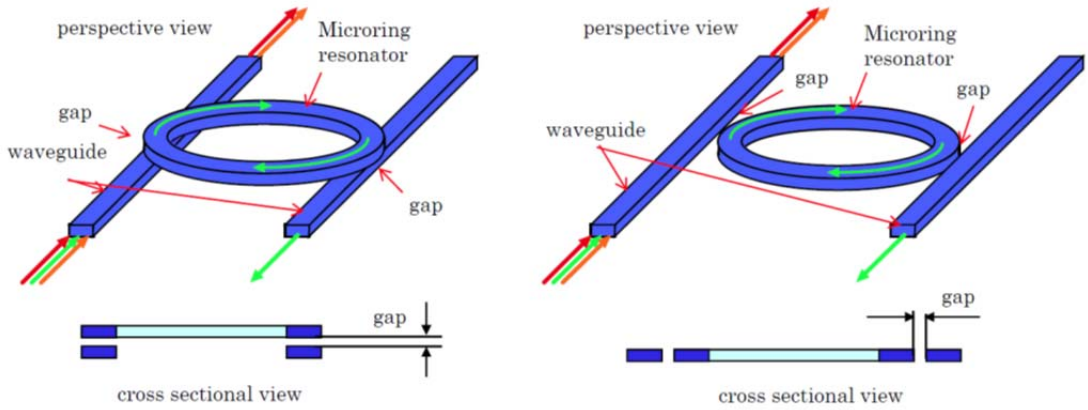
Figure 4-40 Comparison of propagation loss of optical waveguide

4-9-2 Optical coupling

As a method of energy transfer between optical waveguides, there is a method to close a distance between two optical waveguides. The combination of buried optical waveguide in second silicon layer from the surface and rib type or strip type optical waveguide on the surface silicon layer realizes 3 dimensional structures which has coupling in vertical direction.

Figure 4-41 shows the structures of optical coupling with microring resonator. Figure 4-41(a) and (b) is the 3 dimensional structure which is made with pattern SIMOX process and 2 dimensional structure which is made by

existing method, respectively. As pattern SIMOX process creates about 100nm thick BOX layer between surface silicon layer for CMOS circuits and silicon layer for optical circuits, about 100nm thick gap is easily obtained between buried optical waveguide and surface optical waveguide when optical waveguide is fabricated on surface layer as shown in figure 4-41(a). In case of two dimensional structure in which both of two waveguides are on surface silicon, it is difficult to close the distance of two waveguide to 100nm gap as shown in figure 4-41(b).



(a) 3 dimensional structure (b) 2 dimensional structure

Figure 4-41 Comparison of optical coupling with microring resonators

The wavelength filtering characteristics between straight buried waveguide made by pattern SIMOX process and circular shape optical waveguide on surface silicon layer made by etching are shown in figure 4-42. Q value of filtering reaches to 10300. The Q value reaches such a high number of 10300 and filtering function is obtained stably in such a wide range of 50nm, 3 dimensional structure with 100nm thick BOX layer by pattern SIMOX process is indicated to be suitable for stable optical coupling.

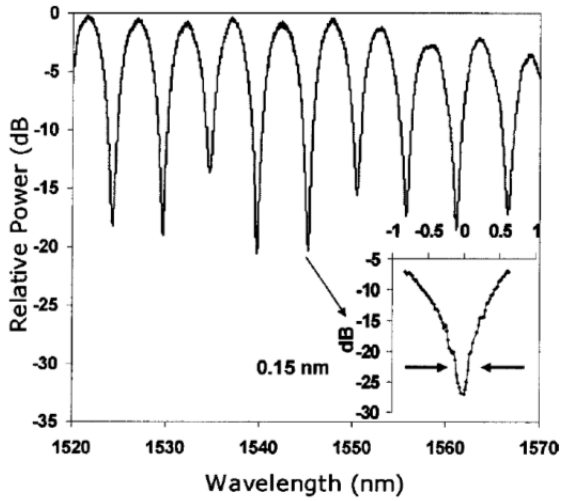


Figure 4-42 Wavelength filtering result with 3 dimensional optical structure by pattern SIMOX[103]

4-9-3 Fabrication of vertically stacked electric and photonic circuits

After fabricating the buried optical waveguide circuits with pattern SIMOX process, MOS transistor is fabricated on the surface layer for CMOS circuits above the silicon layer with buried waveguide [105]. A photograph of the device of MOS transistor and optical circuits are vertically stacked is shown in figure 4-43, and tested result of transistor is shown in figure 4-44 [105]. From this result that both optical circuit and electric device work, the principle of EPIC fabricated pattern SIMOX process is proved.

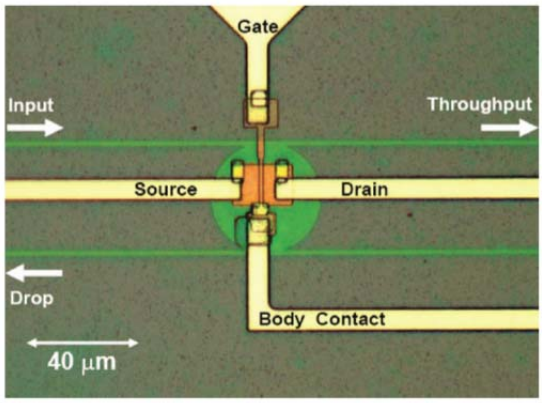


Figure 4-43 Photograph of MOS transistor fabricated above buried optical circuits [105]

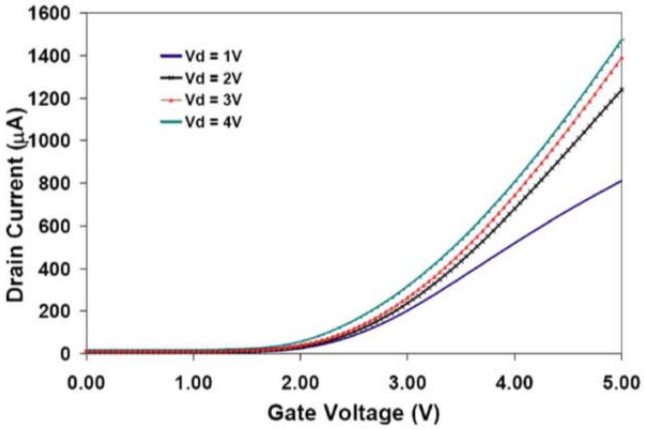


Figure 4-44 Measured characteristics of MOS transistor fabricated above buried optical circuits[105]

4-9-4 EPIC substrate with pattern SIMOX precedes SmartCut

The EPIC substrate described in this chapter is fabricated by the method that pattern SIMOX process is applied to SOI substrate made by SmartCut. The possibility of EPIC substrate fabricated by the method that SmartCut process is applied to substrate with optical circuits by pattern SIMOX is indicated because experimental result that pattern SIMOX realizes tolerable surface flatness. Figure 4-45 shows the structure of EPIC substrate with pattern SIMOX process precedes SmartCut process.

In case that the coupling between optical circuits in second silicon layer for optical circuits and optical circuits or CMOS circuits in surface silicon layer for CMOS circuits layer is emphasized, EPIC substrate described in this chapter is suitable. On the other hand, in case that both optical circuits in second silicon layer for optical circuits and optical circuits or CMOS circuits in surface silicon layer for CMOS circuits layer are used almost independently, EPIC substrate shown in figure 4-45 is suitable.

When the thickness of BOX layer by pattern SIMOX is about 100nm in structure shown in figure 4-45, radiation loss of buried waveguide is not tolerable as discussed with figure 2-9 in chapter 2 but refractive-index modulation devices such as Fresnel optics are adoptable.

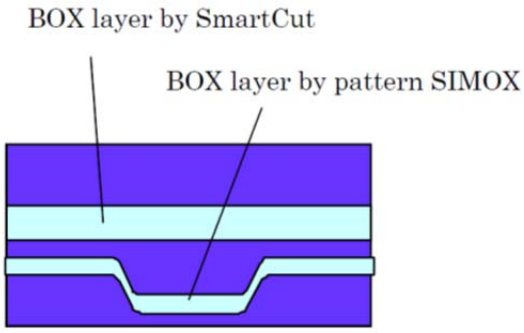


Figure 4-45 EPIC substrate with pattern SIMOX process precedes SmartCut process

4-10 Summary

The fabrication method of silicon layer for CMOS circuits and silicon layer for optical circuits into SOI layer of SOI substrate by making a depth modulated BOX layer with pattern SIMOX process is investigated and described. By this investigation, fabrication condition which keeps defect density of surface silicon layer for CMOS circuits to 7.5 x 10^2/cm^2 and realizes rib type buried optical waveguide in second silicon layer from the surface for optical circuits is obtained. The obtained defect density of 7.5 x 10^2/cm^2 is less than defect density of 1.0 x 10^4/cm^2 which is classified to extremely low defect level in ITRS roadmap issued in 2011 corresponds to 22nm node CMOS design rule.

Through this investigation, the phenomenon that defects are created dominantly where discontinuity of BOX layer by pattern SIMOX even if there is no crack is observed, and requirement of continuous BOX layer to keep surface silicon layer for CMOS circuits in enough quality is presented.

By adapting process simulator of oxygen ion implantation, the relation between transparent mask and projection range and dose density profile is obtained. The reason of asymmetry and separation of BOX layer is proved to be caused from channeling angle when dose is 5.0 x 10^{17}/cm^2 and accelerated voltage is 180keV. The technique of rotating SOI substrate in ion implantation avoids asymmetry and separation of BOX layer is devised and implemented.

In addition, much knowledge related to fabrication of buried optical waveguide beneath the silicon layer for CMOS circuits was obtained such as a protective layer of supply oxygen in 1350 degree C annealing.

Applications and availabilities of buried optical waveguide fabricated by pattern SIMOX are described.

Chapter 5 Optical Memory with using SOI transistor

5-1 Introduction

In chapter 5, an optical device is described which aggressively utilizes two photon absorption phenomena. Transistors fabricated on SOI substrate are very sensitive to floating body effects brought by remaining holes because its body portion is isolated by buried oxide[40]. Some memory devices were reported which detect remaining holes in body portion[106-109]. The principle of these memory devices is impact ionization effects during operation of SOI transistors.

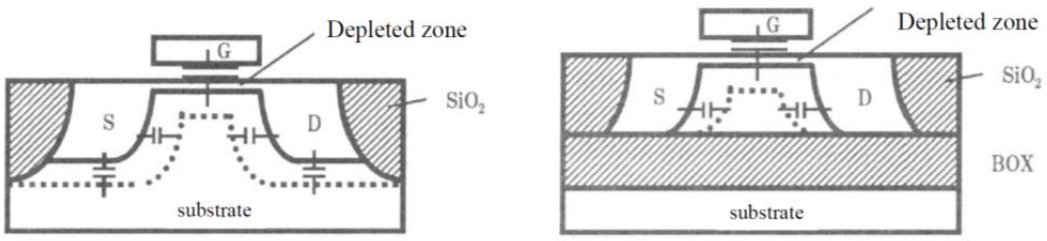
Because silicon is transparent for the light whose wavelength is longer than 1.1μm, it had been believed that propagating light in optical waveguide whose wavelength is 1.35μm or 1.55μm did not affect to SOI transistors. But by existing of two photon absorption phenomena, carriers are created by propagating light in silicon waveguide even if the wavelength is 1.55μm. The amount of carriers reaches to measurable value in case of Raman lasers[110]. In case two photon absorption phenomena by 1.55μm light's illumination on the body portion of SOI transistor creates carriers at measurable value and remaining holes of carriers affect transistor characteristics with floating body effects, there is some possibility of memory devices with SOI transistor.

In this chapter, the optical memory device is described whose principle of recording utilizes the two photon absorption phenomena by 1.55μm light's illumination on the body portion of SOI transistor. At first, the floating body effect on SOI transistors and the memory device with using floating body effects are reviewed. Next, the two photon absorption phenomena in silicon waveguides are introduced. The evaluation results on a possibility of optical memory device through simulations of transistor characteristics with floating body effects caused by carriers created by two photon absorption are shown. In addition, optical memory device fabricated on the pattern SIMOX SOI substrate is shown as an example of functional device in EPIC.

5-2 Floating body effect in SOI transistors

Figure 5-1 shows difference of structure between MOS transistor on bulk silicon substrate and MOS transistor on SOI substrate. By the presence of buried oxide, MOS transistor on SOI(b) has small floating capacitance and small leak current to support substrate. Comparing to MOS transistor on bulk silicon substrate(a), MOS transistor on SOI can be operated at higher frequency and has lower power consumption. But from the reason that body portion is floated, the body portion has influences from bias voltage of circumference, operating history of transistor, or others. The general name of phenomena caused by the influences is floating body effects [40].

Although there are many phenomena in floating body effects, two selected effects will be reviewed in this section. One is kink effect which appears in drain current-drain voltage relationship [111]. Second is history effect which makes destabilizing influence on threshold voltage [112].



(a) (b)

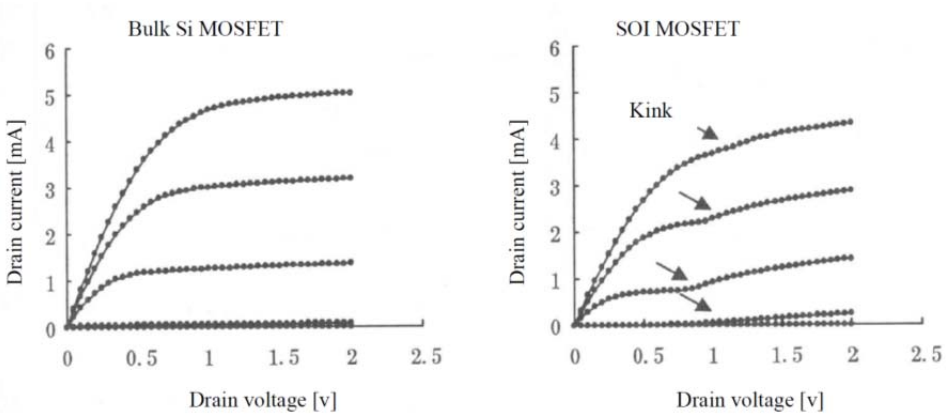
Figure 5-1. Structures of (a) Si MOSFET and (b) SOI MOSFET

5-2-1 Kink effect in drain current-drain voltage relationship

Figure 5-2 shows drain current(I_d)-drain voltage(V_d) relationship of Si MOSFET fabricated on bulk silicon substrate and Si MOSFET fabricated on SOI substrate[40]. The kink effect is a changing of gradient in I_d- V_d characteristics. The principle of kink effect is shown in figure 5-3. When increasing the drain

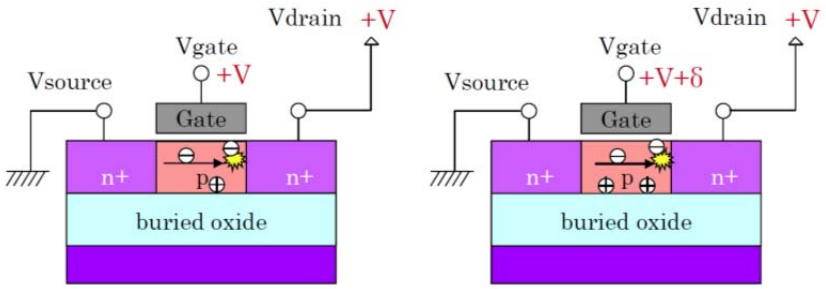
voltage, electrons with higher energy collide with silicon atoms in body portion and this colliding creates carrier. This carrier creation phenomenon by the colliding is called impact ionization and is in both bulk Si MOSFET and SOI MOSFET.

In case of SOI MOSFET, remaining holes which have slower velocity than electrons increase by impact ionization as shown in Figure 5-3 (a). Increasing holes which have plus voltage at the body portion is the same with increasing bias voltage, so this effect reduces threshold voltage of MOSFET and increases gate voltage to V+δ as shown in Figure 5-3 (b). As a result, drain current is increased and impact ionization phenomena are increased additionally. Finally, the changing of gradient in I_d- V_d relationship (Kink effect) is observed. However Kink effect is regarded a benefit in the aspect of increasing the drain current, Kink effect makes a model complex and is regarded as a problem in circuit design.



(a) bulk Si MOSFET (b) SOI MOSFET

Figure 5-2. Drain current(I_d) – drain voltage(V_d) relationship [40].



(a) (b)

Figure 5-3. Kink effect caused by impact ionization.

(a) carrier generation by impact ionization

(b) positive feedback in drain current by remaining holes at body portion

5-2-2 Instability of threshold voltage by history effect

History effect is an effect that remaining holes created by impact ionization affect the next transistor operation. Because remaining holes at the body portion are regarded as a plus bias voltage, the transistor with remaining holes has smaller threshold voltage than the transistor with no remaining holes.

Assaderaghi observed variation of threshold voltage by history effect with measuring the delay time of transistor with changing the frequency of repeat transistor operations [112]. The result on history effect by Assaderaghi is plotted in figure 5-4. This result shows that the delay time of repetitive operation with longer interval time than 10^{-2}sec. is same with single pulse input operation. The delay time of repetitive operation with shorter interval time than 10^{-2}sec. is different from single pulse input operation

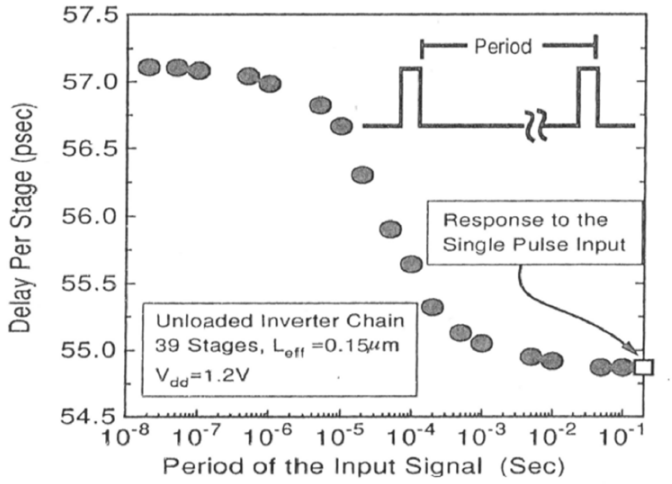


Figure 5-4. Experimental results of history effect [112].

5-3 Memory device whose recording principle is impact ionization

Current low-cost DRAM memory device is the capacitor type memory whose shape is deep hole fabricated on bulk Si substrate. From the reason that the capacitor type memory device with deep hole cannot be made on SOI substrate, Sallese and Matsumoto proposed and demonstrated memory device with history effect (floating body effect) on SOI substrate [106-109].

Figure 5-5 shows the principle of recording and holding state of memory device with floating body effect. Figure 5-5 (a) and (b) are regarding having data "1". Figure 5-5(a) shows recording method that makes remaining holes at the body porting by impact ionization. Figure 5-5(b) is the state of data "1" that there is remaining holes at body portion. Figure 5-5 (c) and (d) are regarding having data "0". Figure 5-5(c) shows erasing method that sweeps the remaining holes to the drain by applying a minus voltage. Figure 5-5(d) is the state of data "0" that there are no remaining holes at body portion.

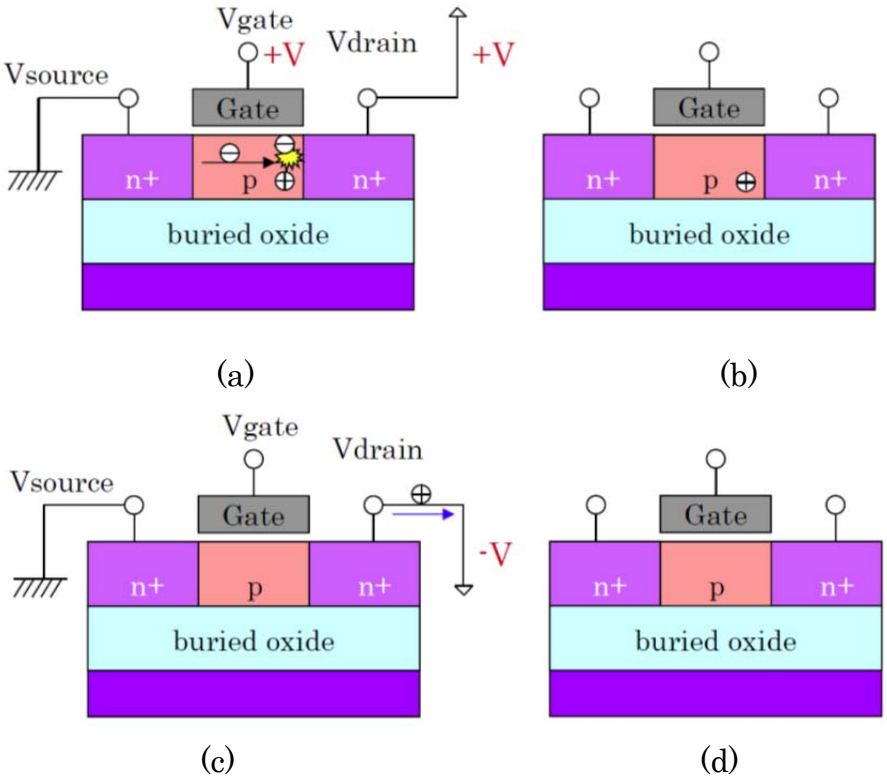


Figure 5-5. Recording methods and states of memory device.

The reading method of this device is shown in figure 5-6. This method utilizes monitoring of drain current at the time when the input pulse is applied to drain terminal of the transistor to distinguish between state of data “1” and state of data “0” [113]. In case there is remaining holes, state “1”, threshold voltage of transistor is smaller than the case there is no remaining holes, state “0”, so delay time of transistor is shorter. As a result, larger drain current is to be sensed at fixed point of time in case there is remaining holes, state “1”. This method is proposed by Okhonin as a method of measuring the remaining holes at body [114].

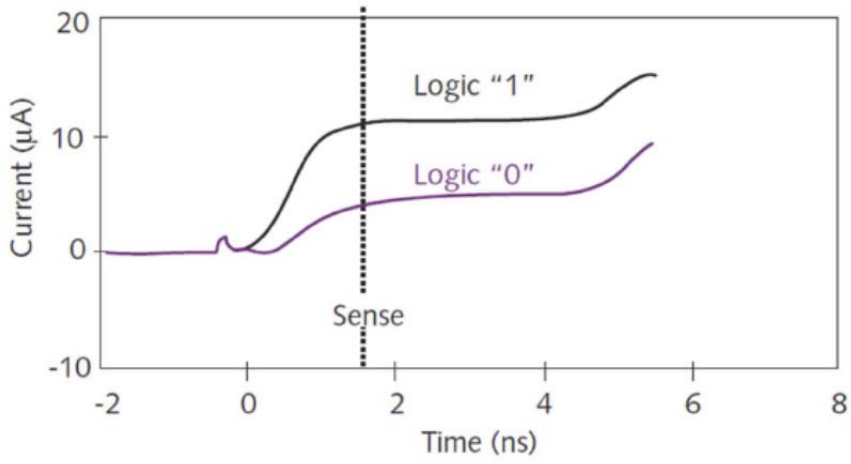


Figure 5-6. Method of reading the memory[113].

5-4 Memory device with two photon absorption

Two photon absorption phenomenon in silicon waveguide is the nonlinear effect related to a light with doubled frequency. The wavelengths of doubled frequency of 1.35μm and 1.55μm light are 0.675μm and 0.775μm, respectively, which are opaque for silicon, so the light with doubled frequency is absorbed in silicon waveguide. This phenomenon is noticeable when large power of light is propagating in low propagating loss waveguide. Soref reported that the carriers created by two photon absorption brought photon absorption and index change of silicon [115]. The photon absorption phenomenon caused by two photon absorption is called as free carrier absorption (FCA) [116,117].

In the field of silicon Raman laser, treatment of FCA is important [110, 118]. Jalali demonstrated silicon Raman laser by avoiding FCA with applying short pulse laser [119]. Paniccia demonstrated continuous silicon Raman laser by electrically sweeping the carriers with applying pin type structure waveguide as shown in figure 5-7 [21].

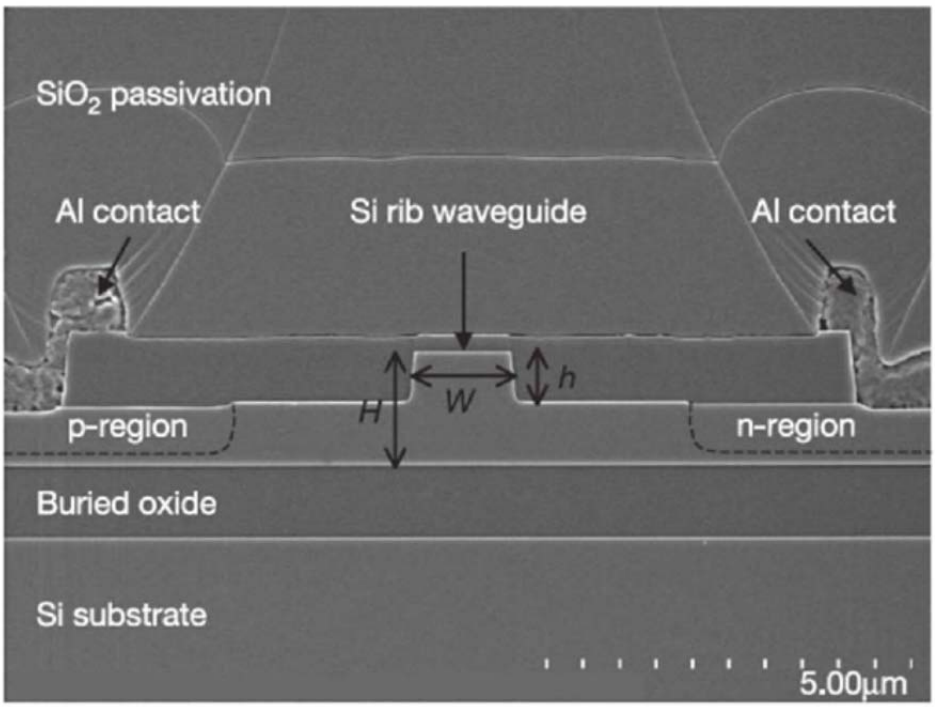


Figure 5-7. Pin type waveguide structure for silicon Raman laser [21].

The pin type waveguide structure can sweep the carriers by applying the voltage, so sweeping carrier became controllable. This pin type waveguide enables optical modulator [120], variable optical attenuator (VOA) [121]. In addition, energy picking up devices which utilize the current of sweeping carriers as energy are reported [122, 123].

Regarding analyzing the amount of carriers caused by two photos absorption, TPA coefficient β which is a coefficient of generating the carriers as a function of energy of the light is reported in some references [124-126]. The recombination of carriers and mobility of holes and electrons in silicon waveguide are reported by Jalali [127, 128]. Jalali used semiconductor device simulator and their TPA coefficient β was 0.7 cm/GW.

In this section, the influence of carrier generation caused by two photon absorption to SOI transistor is evaluated with semiconductor device simulator, and optical memory device made of SOI transistors whose recording method is two photon absorption, is examined.

5-4-1 Simulation model

Atlas device simulation tool made by SILVACO is used to estimate the influence for transistor characteristics by carrier generation caused by two photon absorption. This is the same tool by which Jalali reported the recombination of holes and electrons [127] and sweeping carriers by applying the voltage to pin type waveguide [128].

The model structure is shown in figure 5-8. This npn type SOI transistor is the basic model structure prepared for calculating floating body effect in Altas library. This is also partially-depleted (PD) type SOI transistor [40]. N doping density of source and drain is $1.0 \times 10^{20}/cm^3$ and p doping density of body is $1.0 \times 10^{17}/cm^3$. The gate length is 1.0μm and length of the device in simulation is 3.0μm. Both of thickness of buried oxide and thickness of SOI are 0.3 μm. Thickness of gate oxide is 17nm. The light is uniformly illuminated only on body portion which size is 0.3μm x 1.0 μm. The carrier density caused by two photon absorption is expressed to $\beta I^2_p/2E_p$, with using Optical power density I_p, plank constant E_p, and TPA coefficient β. The value of TPA coefficient β is 0.7/GW as wavelength of light is 1.55μm [128].

In simulation, carrier at certain value corresponds to light power is filled as initial state, then, stable state is calculated after carrier recombination and moving of holes and electrons. The drain voltage was applied at the end of initial state. Therefore the moment at time of 0 in the drain voltage profile is at the end of initial state. The drain voltage function is sinus function whose frequency is 1kHz and amplitude is 2V. So, the drain voltage is changed from 0V -> 2V -> 0V. The gate voltage was set to 0.2V constantly.

Because the simulation structure is two dimensional, the width of device was set to 1cm as a simulation unit. In case the actual gate width is 10μm, the drain current is needed to be divided by 1000.

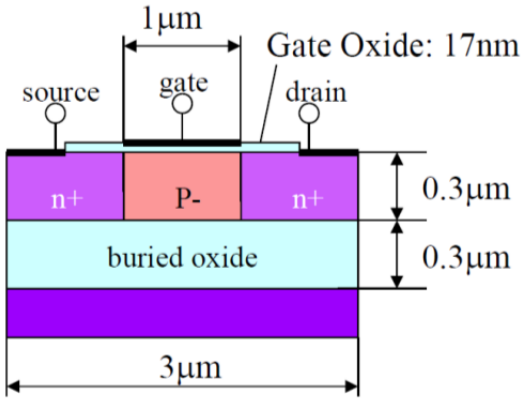


Figure 5-8. Simulation structure of SOI transistor.

5-4-2 Simulation results

The calculated drain current is shown in figure 5-9. There are three illumination parameters in light illumination which are 0.51mW, 4.68mW, and 0W (no illumination). This result shows that drain current of two illumination case of 0.51mW and 4.58mW have apparently larger than the current of no illumination. So it indicates that the carrier caused by two photon absorption has some effects which decrease the threshold voltage as same as history effect of floating body effect.

The drain currents at 1.0V, 1.25V, and 1.5V in the step of increasing drain voltage are plotted in figure 5-10 as a parameter of illumination power. From figure 5-10, drain current at 1.0V, 1.25V, and 1.5V are changed at 0.5mW illumination like as step function. It shows that the floating body effect is not observed under 0.5mW illumination. The boundary of floating body effect is 0.5mW in case body portion is 0.3μm x 1.0μm, this illumination power corresponds to 1.67mW/μm^2. This value is threshold power of recording of optical memory device. The criterion value of drain current can be set to 5nA at the drain voltage is in the range from 1V to 1.5V. In case the drain current is more than 5nA when the drain voltage is from 1V to 1.5V, it is distinguished that data is recorded with larger illuminating power than threshold power.

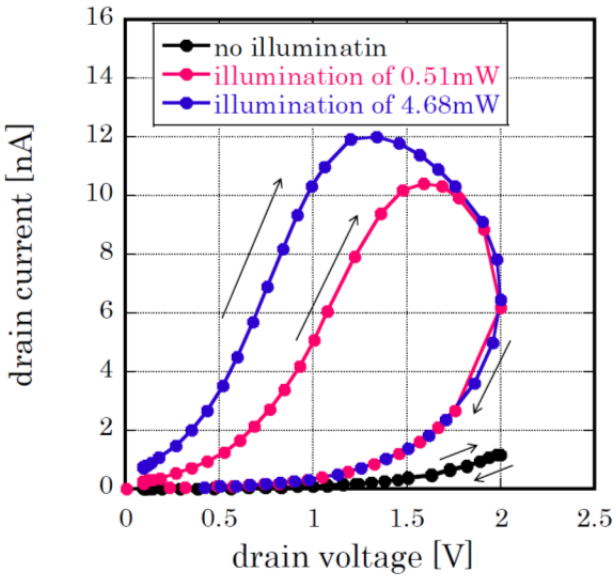


Figure 5-9. Drain current – drain voltage characteristics of optical memory.

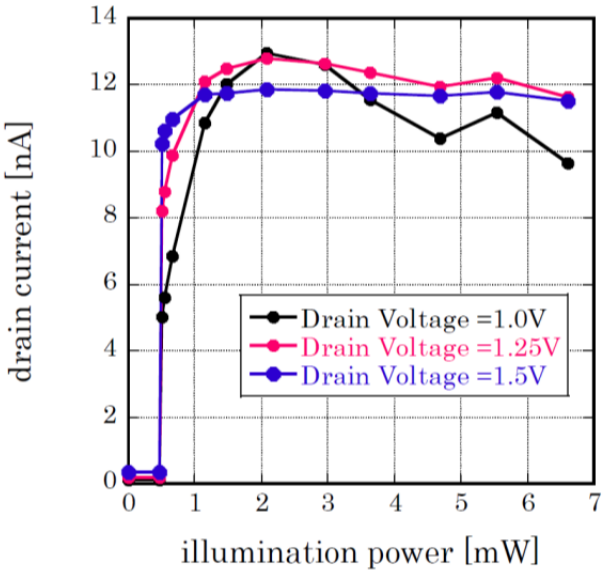


Figure 5-10. Light power dependence of drain current at fixed drain voltage.

The retention characteristics of SOI transistor memory are discussed. Figure 5-11, 12 shows density of hole at body portion along with time when illumination power is 1.5mW. In these figures, the start points (t=0) are the end point of light illumination, and plotting values are the average of hole densities in body portion. From figure 5-11, it takes about 1 second until hole density reaches

to stable value with gate voltage of 0.2V. Figure 5-12 shows that drain current at 1μsec reached to 27nA.

The required time that hole density reaches to stable value is the function of gate length because the velocity of hole is fixed by doping density. Therefore if the gate length is reduced to 1/10, the time that hole density reaches to stable value is also reduced to 1/10. For the current SOI transistor whose gate length is 45nm or 32nm, the time that hole density reaches to stable value is still several tens msec. As a result, the retention characteristics of this memory is several tens msec. If memory user wants to have longer retention time than several tens msec, refresh procedure which is used in DRAM is required. From the reason that the structure of this memory is same with floating body memory whose recording principle is impact ionization, refresh method for floating body memory [129] can be applied.

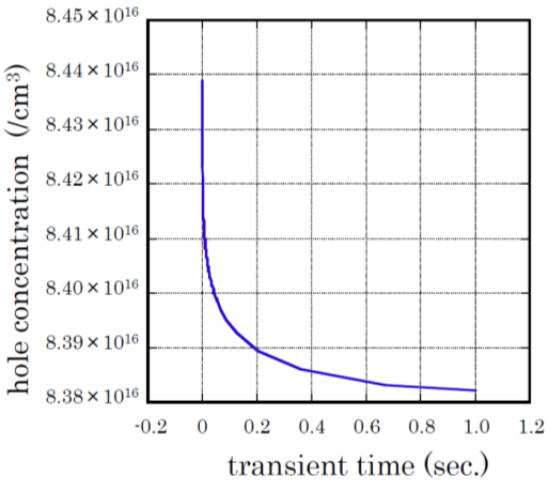


Figure 5-11. Hole density characteristics at body portion.

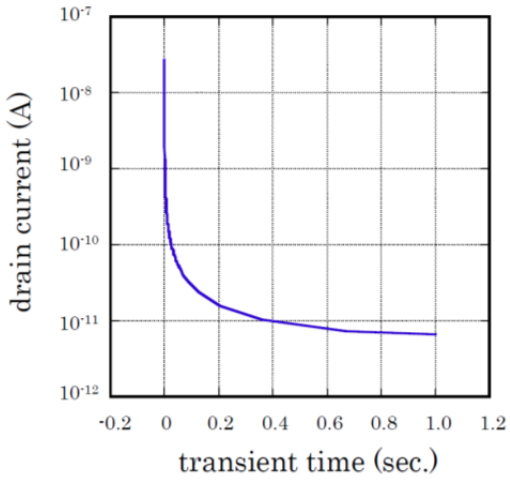


Figure 5-12. Drain current characteristics.

Drain currents at reading step when transistor operating frequency is varied 1kHz, 1MHz, 50MHz, and 250MHz are plotted in figure 5-13. The other parameters written in these figures are the same with figure 5-9 and 5-10.

As increasing the frequency, the difference of drain current between with light illumination and without illumination becomes large. The maximum difference of drain current as explained in figure 5-13(a), is plotted in figure 5-14. From these figures the history effect caused by two photon absorption becomes remarkable as increasing the frequency. Considering the results in figure 5-11, the result that remarkable difference at higher frequency seems to be brought from the transistor operation is performed under the higher carrier density.

As Assaderaghi's result plotted in figure 5-4 shows that shorter operation interval has larger history effect, the history effect caused by two photon absorption has same characteristics that immediate operation after illumination has larger history effect.

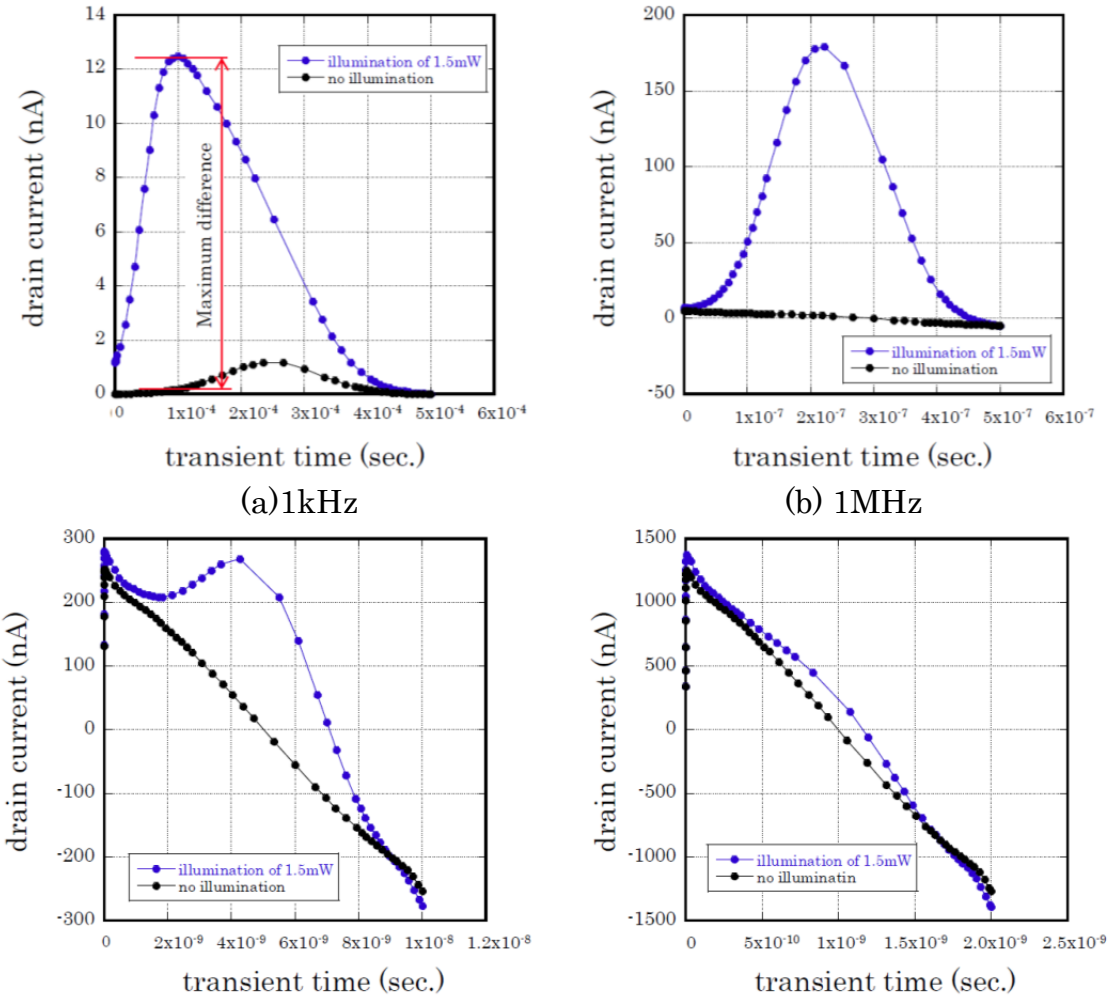


Figure 5-13. Characteristics of SOI transistor optical memory.

(frequency dependence at read step)

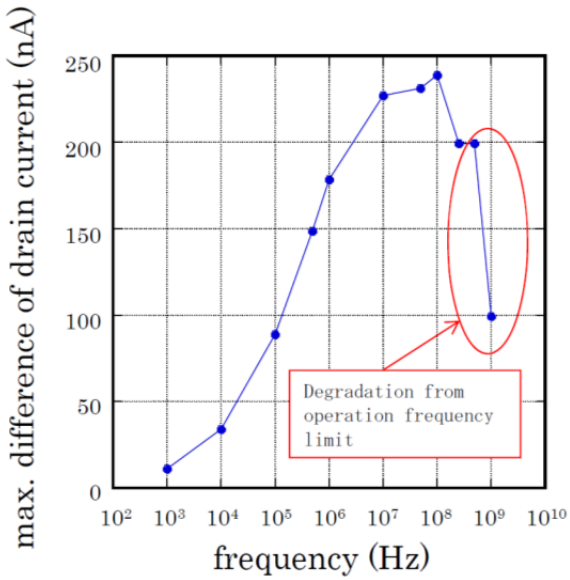


Figure 5-14. The maximum difference of drain current at reading step.

5-5 Operation of SOI transistor optical memory

In this section, operation method of SOI transistor optical memory whose possibility was examined in previous section is discussed.

The operation steps are shown in figure 5-15. The operation step can be selected by changing drain voltage as shown in figure 5-15(a). Firstly, sweeping remaining holes at body portion is performed as a reset (erase) step before light illumination. This reset step is the same with the reset step of floating body memory shown in figure 5-5(c). The reset step is to apply minus voltage on drain terminal. Next step is recording step. Refer to simulation results of previous section, at recording step, the light power with over thresholds power is illuminated on body portion of optical memory to keep remaining holes caused by two photon absorption. At this step drain voltage is kept to 0V. At reading step, drain current is monitored under the condition that drain voltage is changed as 0V -> 2V -> 0V (V_{read} = 2V). And at the fixed point on increasing the drain voltage, the value of drain current is compared to criterion value. When the drain current

at the fixed time is larger than criterion value, the memory data was judge to “1”. At all steps gate voltage is kept to 0.2V.

For example as shown in figure 5-15(b), in case drain voltage is changed to 0V -> 2V -> 0V at 1kHz and drain current at drain voltage is 1.25V is larger than 5nA (criterion value), we obtain that there were enough remaining holes at body portion before applying voltage and light with over threshold power was illuminated. For next example as shown in figure 5-15(c), in case drain current at drain voltage is 1.25V is smaller than 5nA (criterion value), we obtain that there were not enough remaining holes at body before applying voltage and light with over threshold power was not illuminated.

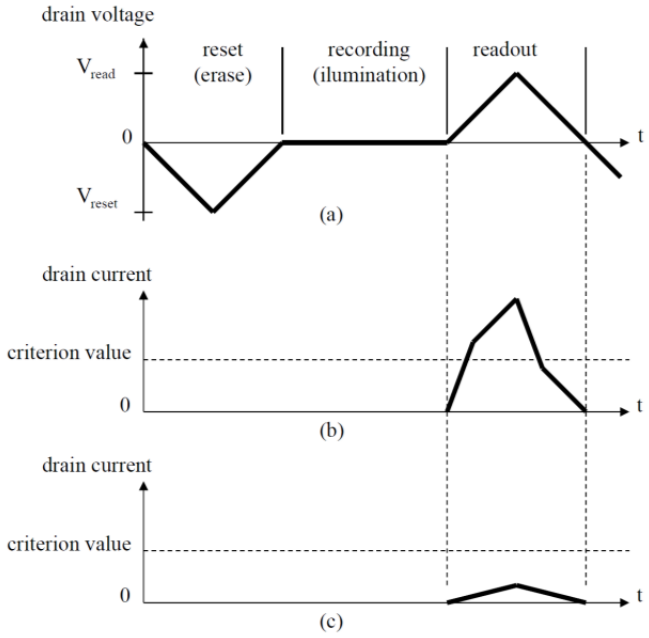


Figure 5-15. Operation steps of SOI transistor optical memory.

5-6 Configuration of SOI transistor optical memory

The configuration of SOI transistor optical memory whose data is recorded by light illumination through optical waveguide is discussed in this section. The example of device structure of optical memory on EPIC substrate made by pattern

SIMOX process is shown in figure 5-16. In this example, optical waveguide is located just under the optical memory made of SOI transistor, and optical waveguide is parallel to body of the transistor. The optical power distribution on body portion of transistor was calculated by optical waveguide simulator (FIMMWAVE by Photon Design). Figure 5-17 shows detail structure of the device for optical simulation. The structure is the combination of optical waveguide which is examined with experiments in previous chapter shown in figure 4-5 and SOI transistor which is evaluated as optical memory shown in figure 5-8. In this structure, ITO (Indium Tin Oxide) is used as an electrode instead of poly silicon in order to increase the illumination power on body portion. Although normal transistor in CMOS circuits uses poly silicon which has lower electric resistance and has optical absorption as a gate electrode, there is no need to use lower electric resistance as gate electrode because applied gate voltage in SOI transistor optical memory is stable. So it is possible to use ITO which has electric resistance and transparent as gate electrode. The index of ITO for light of 1.55μm wavelength is about 1.8 [130], ITO increases the power distribution on the body portion because of lower index than poly silicon.

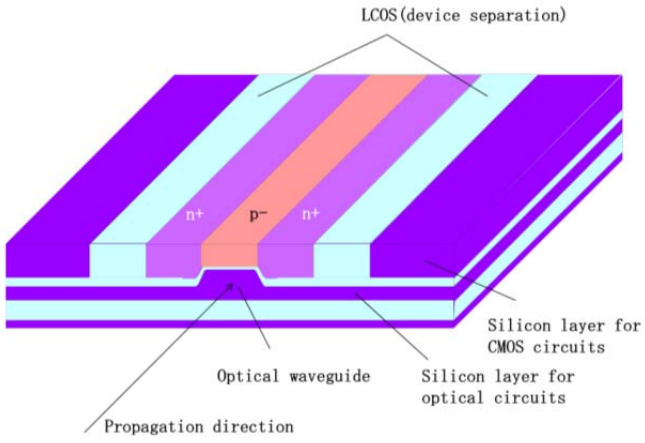


Figure 5-16. Configulation of SOI transistor and optical waveguide.

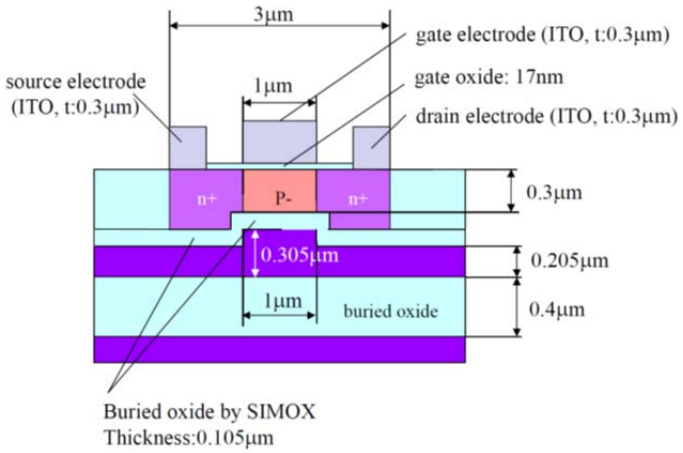


Figure 5-17. Device structure in optical simulation of optical memory by SOI transistor.

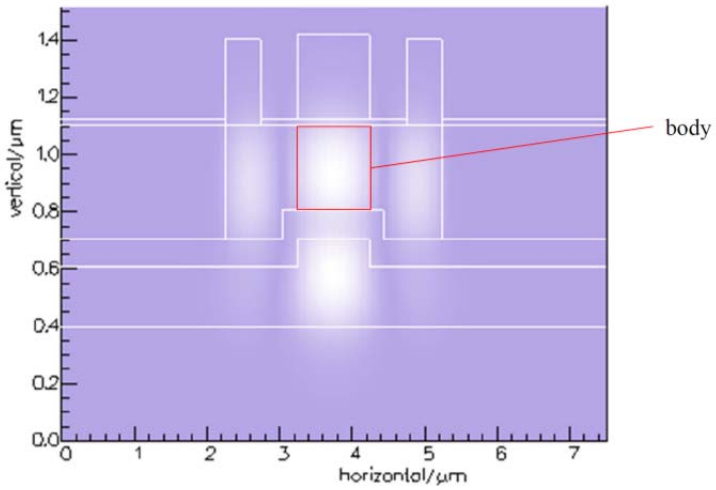


Figure 5-18. Simulation results of electric field distribution.
(wavelength 1.55μm, TE mode).

At the calculation of electric field and propagation loss, absorption constant α of doped areas in SOI transistor are shown in the followings. At source and drain portion whose doping value is 1 x 10^{20}/cm^3, α is 9.53 for 1.55μm light from the reference by Soref [6]. At body portion whose doping value is 1 x 10^{17}/cm^3, α is 0.154 from the reasons that α is stable when doping density is lower than 7 x 10^{17}/cm^3 reported by Strum [131] and propagation loss of ridge waveguide in 3 x 10^{16}/cm^3 doping area was 6.7dB/cm for 1.55μm light reported by Liu [132]. α of

0.154 is calculated from propagation loss of 6.7dB/cm.

The simulated electric field distribution by FIMMWAVE is shown in figure 5-18. This figure indicates that light propagation through SOI transistor optical memory is possible. The calculated propagation loss of the device is 2.25dB/cm. When the device length is set to 10μm, optical absorption of the device is 0.104%. The amount of this absorption loss is negligible. The calculated energy distribution in the body portion is 31.1%.

The data recording to SOI transistor optical memory can be performed with more than 0.5mW light illumination to the body portion. With the consideration of 31.1% power distribution to the body portion and 0.104% power loss for 10μm length device, 1.61mW is required as a minimum propagating power in optical waveguide to have more than 0.5mW light illumination on body portion at the end of optical device.

As a feature of EPIC substrate in this research, light illumination from substrate side of the SOI transistor is effective method of illumination for avoiding electrodes because it is difficult to avoid electrodes with many layers in case of light illumination from top side of SOI transistor. In addition, by applying the optical waveguide parallel to body portion as shown in figure 5-16, effective light illumination can be obtained.

The light illumination to optical memory can be controlled by using optical switch [133] or optical light modulator [24]. Figure 5-19 shows the example of light control device which consists microring resonator type optical light modulator reported by Lipson[23].

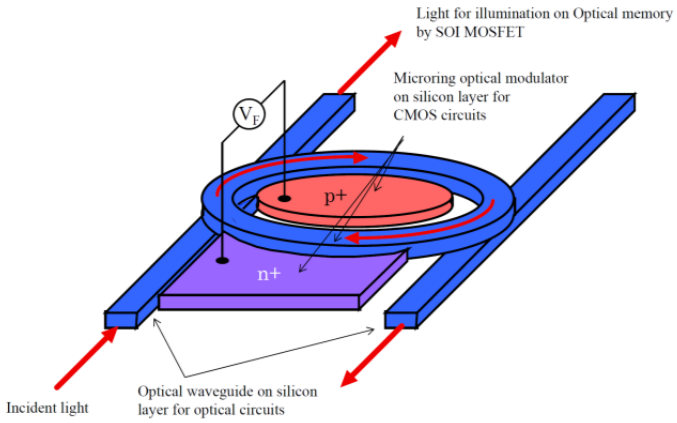


Figure 5-19. Example of light illumination control device.

5-7 Summary

The possibility of optical memory device with SOI transistor is evaluated. The principle of the optical memory is carrier generation by two photon absorption with 1.55μm wavelength light at body portion of SOI transistor, and remaining holes at body portion decrease thresholds voltage at next transistor operation as same as history effects in floating body effects. The result that more than 0.5mW light illumination to body portion whose size is 0.3μm x 1.0μm (1.67 $mW/\mu m^2$) reduces thresholds voltage at next transistor operation by floating body effect is simulated. The required optical power for recording is attainable value.

As an example of functional device on EPIC substrate by pattern SIMOX, the optical memory device which is combination of buried optical waveguide and SOI transistor located above the buried waveguide is examined. The required light illumination power in optical waveguide was calculated to 1.61mW.

Chapter 6 Conclusion

6-1 Summary

The purpose of this research is to realize EPIC substrate which has vertically stacked surface silicon layer for CMOS integrated circuits and silicon layer for optical circuits as an optical waveguide technology which is compatible with CMOS integrate circuits technologies. This EPIC technology is expected technology to bring high functionality and low cost simultaneously, especially for short distance optical communication.

The method of fabrication of buried optical waveguide by pattern SIMOX with keeping surface silicon layer enough quality for CMOS integrated circuits is proposed and proved. As a required technology for practical use of EPIC substrate, non-destructive defect examination method which pinpoints layer where defect exists effectively is proposed and verified. In addition, SOI transistor memory device which utilizes interaction between vertically stacked SOI transistor and optical waveguide is proposed and evaluated.

The obtained results through this research are written in the followings.

1. With the experiment of uniform SIMOX on flat SOI substrate, creation of uniform thickness and flat BOX layer in SOI layer is observed, and the surface silicon layer for CMOS integrated circuits has good quality in defect density which is classified to extremely low defect level in ITRS roadmap issued in 2011 corresponds to 22nm node CMOS design rule.
   (a) In silicon layer for optical circuits, some defects observed at the density that does not affect property of optical circuits but affects property of CMOS electrical circuits.
   (b) The necessity of a simplified non-destructive defect evaluation method which pinpoints the layer where defect exists is clearly shown.

2. As a method which pinpoints defect position, non-destructive defect examination method using fluorescent microscope consists two exposures which pinpoints 3D position of defect is proposed and verified.
   (a) Through the verification experiment with fluorescent beads placed on the specimen with groove structure, the proposed method has 0.1μm and 30nm resolution in air and in silicon, respectively. The proposed defect examination method which reduces to 1/10 in required data storage size is so effective that it is adaptable to one hundred percent inspection.

3. A method of fabricating optical waveguide in second silicon layer from the surface by pattern SIMOX technology is proposed and proved with keeping enough quality of surface silicon layer for CMOS electrical circuits.
   (a) By process modification of mask thickness, dose value, anneal condition, and rotation in ion implantation, fabrication condition of continuous and symmetrical BOX structure with depth modulation is obtained using mass production equipment. The fabrication of EPIC substrate which is compatible to CMOS electrical circuits is proved.
   (b) The phenomenon that defects are created dominantly at discontinuity of BOX layer by pattern SIMOX even if there is no crack is observed. The requirement of continuous BOX layer to keep surface silicon layer for CMOS circuits in enough quality is presented.
   (c) The defect density of surface silicon layer for CMOS circuits of 7.5 x $10^2/cm^2$ and realizes rib type buried optical waveguide in second silicon layer for optical circuits is obtained. The obtained defect density of 7.5 x $10^2/cm^2$ is less than defect density of 1.0 x $10^4/cm^2$ which is classified to extremely low defect level in ITRS roadmap issued in 2011 corresponds to 22nm node CMOS design rule.

4. The possibility of SOI transistor optical memory is evaluated. The principle of evaluated device is carrier generation by two photon absorption with 1.55μm

wavelength light at body portion of SOI transistor, and remaining holes at body portion decrease thresholds voltage at next transistor operation as same as history effects in floating body effects.

(a) The analyzed result is more than 1.67 mW/μm^2 light illumination on body portion of SOI MOSFET with SOI thickness of 0.3μm and gate length of 1μm reduces thresholds voltage at next transistor operation by floating body effect. The reduction of thresholds voltage increases drain voltage with 10 – 200nA, so possibility of memory device is proved.

(b) As an example of functional device on EPIC substrate by pattern SIMOX, the optical memory device which is combination of buried optical waveguide and SOI transistor located above the buried waveguide was examined. The required light illumination power in optical waveguide was calculated to 1.61mW which is attainable value.

6-2 Future work

This research proves optical circuit allocation in different layer with CMOS electrical circuits, increasing the area of CMOS chip by adding optical circuits can be minimized.

The different layer allocation of optical circuits and CMOS electrical circuits releases the requirement of coincide the thicknesses of silicon layer for optical circuits and silicon layer for CMOS circuits. Because thickness of silicon layer is to be reduced as design node of transistor is reduced, release of the requirement of coincide the thicknesses of silicon layer for optical circuits and silicon layer for CMOS circuits gives the chance of universal design of optical circuits independent of CMOS design node. CMOS designer is able to bring forward design node and also adopt FDSOI with 60-80nm SOI of FINFET without waiting the design progress of optical circuits design.

The different layer allocation of optical circuits and CMOS electrical

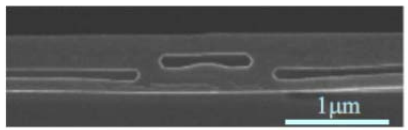
circuits also allows the wider area for optical circuits. Therefore optical device which requires wider area such as arrayed waveguide grating (AWG) can be applied.

A simplified non-destructive defect examination method which pinpoints 3D position of defect is suitable to find low frequency event with fluorescent microscope. Therefore application of this method is not fixed to find defects. Other applications such as genetic screening are possible.

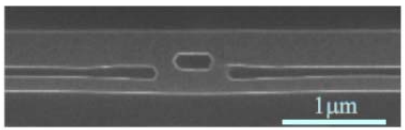
However there are many challenges before practical use of silicon photonics and EPIC substrate, I wish this research would be an opportunity of practical use of silicon photonics and EPIC substrate.

Appendix

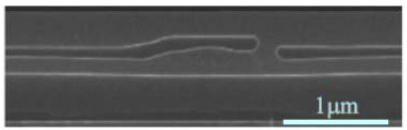
Appendix figure 1-1 cross sectional observation (mask width: 0.5μm)



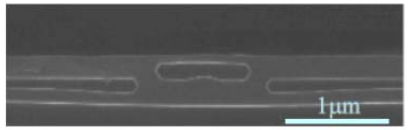
(a-1) mask thick 150nm ,non ITOX, without LTO



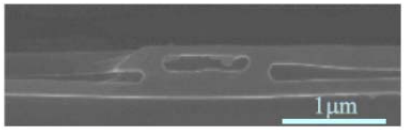
(b-1)mask thick 125nm, non ITOX, without LTO



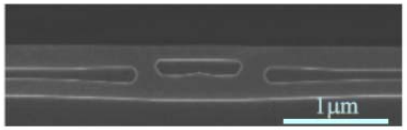
(c-1)mask thick 100nm, non ITOX, without LTO



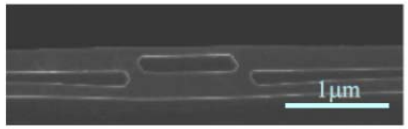
(a-2)mask thick 150nm , slight ITOX, without LTO



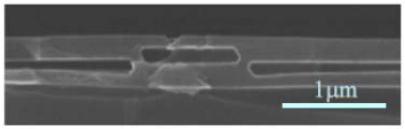
(b-2)mask thick 125nm, slight ITOX, without LTO



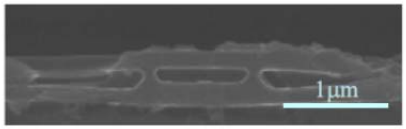
(c-2)mask thick 100nm, slight ITOX, without LTO



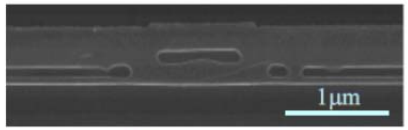
(a-3)mask thick 150nm , normal ITOX, without LTO



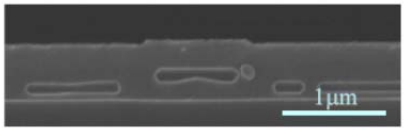
(b-3)mask thick 125nm, normal ITOX, without LTO



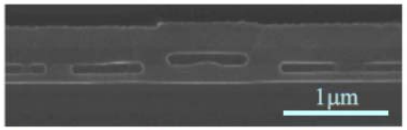
(c-3)mask thick 100nm, normal ITOX, without LTO



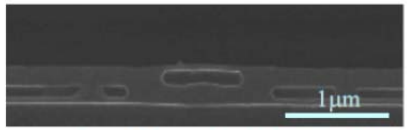
(a-4)mask thick 150nm , non ITOX,LTO



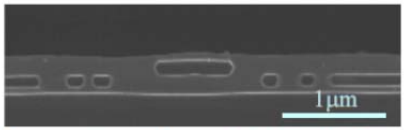
(b-4)mask thick 125nm, non ITOX,LTO



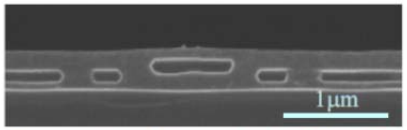
(c-4)mask thick 100nm, non ITOX,LTO



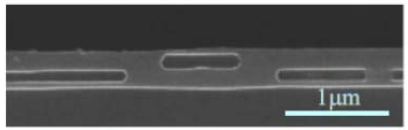
(a-5)mask thick 150nm , slight ITOX,LTO



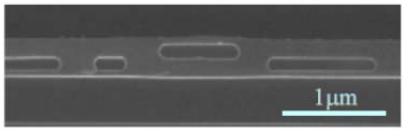
(b-5)mask thick 125nm, slight ITOX,LTO



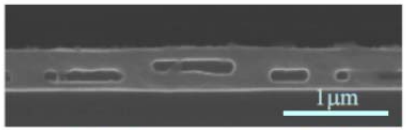
(c-5)mask thick 100nm, slight ITOX,LTO



(a-6)mask thick 150nm , normal ITOX,LTO

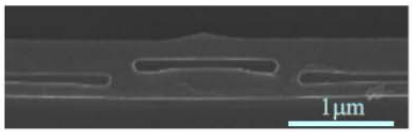


(b-6)mask thick 125nm, normal ITOX,LTO

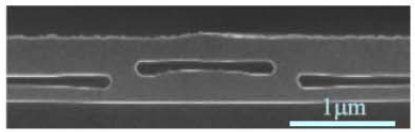


(c-6)mask thick 100nm, normal ITOX,LTO

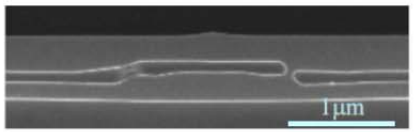
Appendix figure 1-2 cross sectional observation (mask width: 1.0μm)



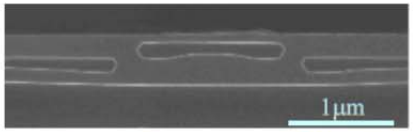
(a-1) mask thick 150nm ,non ITOX, without LTO



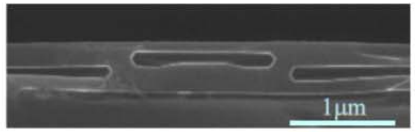
(b-1)mask thick 125nm, non ITOX, without LTO



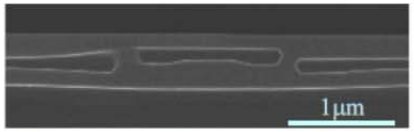
(c-1)mask thick 100nm, non ITOX, without LTO



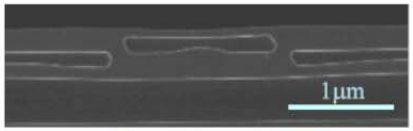
(a-2)mask thick 150nm , slight ITOX, without LTO



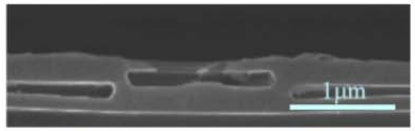
(b-2)mask thick 125nm, slight ITOX, without LTO



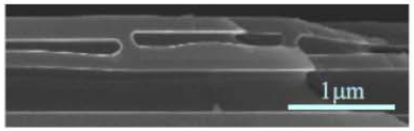
(c-2)mask thick 100nm, slight ITOX, without LTO



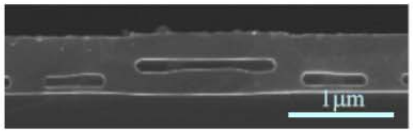
(a-3)mask thick 150nm , normal ITOX, without LTO



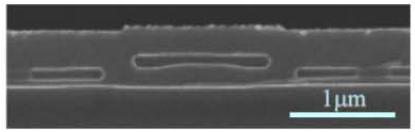
(b-3)mask thick 125nm, normal ITOX, without LTO



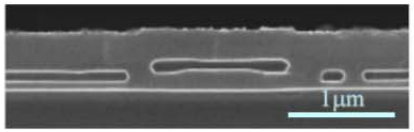
(c-3)mask thick 100nm, normal ITOX, without LTO



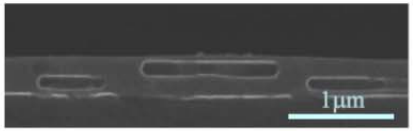
(a-4)mask thick 150nm , non ITOX,LTO



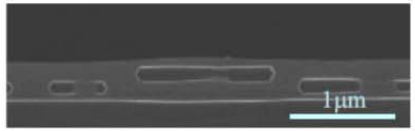
(b-4)mask thick 125nm, non ITOX,LTO



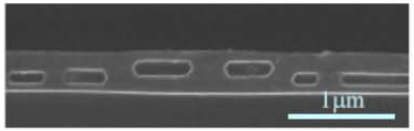
(c-4)mask thick 100nm, non ITOX,LTO



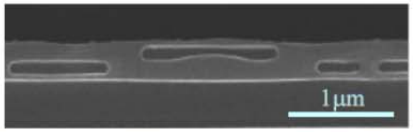
(a-5)mask thick 150nm , slight ITOX,LTO



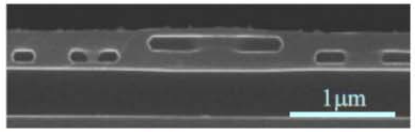
(b-5)mask thick 125nm, slight ITOX,LTO



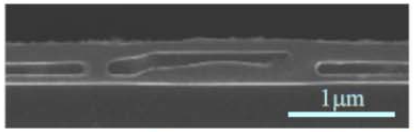
(c-5)mask thick 100nm, slight ITOX,LTO



(a-6)mask thick 150nm , normal ITOX,LTO

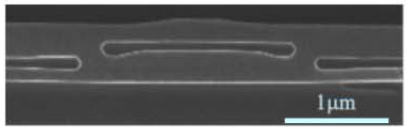


(b-6)mask thick 125nm, normal ITOX,LTO

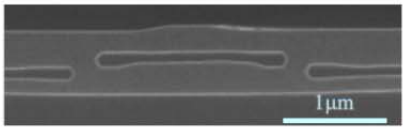


(c-6)mask thick 100nm, normal ITOX,LTO

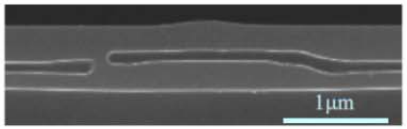
Appendix figure 1-3 cross sectional observation (mask width: 1.5μm)



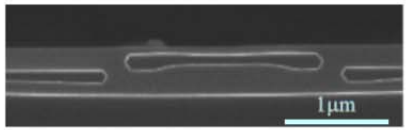
(a-1) mask thick 150nm ,non ITOX, without LTO



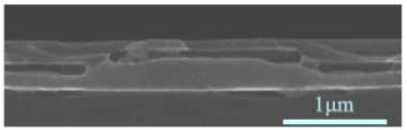
(b-1)mask thick 125nm, non ITOX, without LTO



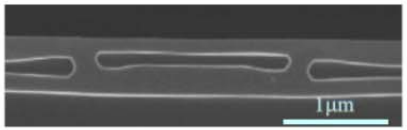
(c-1)mask thick 100nm, non ITOX, without LTO



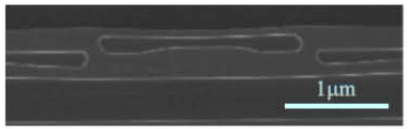
(a-2)mask thick 150nm , slight ITOX, without LTO



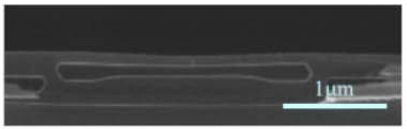
(b-2)mask thick 125nm, slight ITOX, without LTO



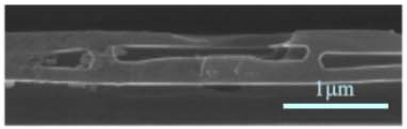
(c-2)mask thick 100nm, slight ITOX, without LTO



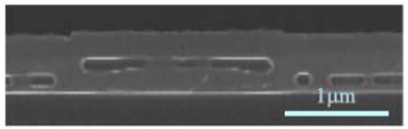
(a-3)mask thick 150nm , normal ITOX, without LTO



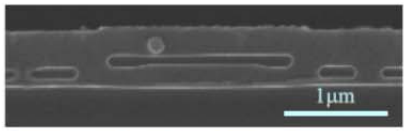
(b-3)mask thick 125nm, normal ITOX, without LTO



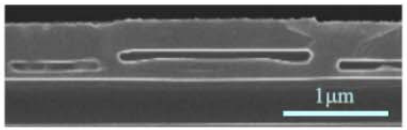
(c-3)mask thick 100nm, normal ITOX, without LTO



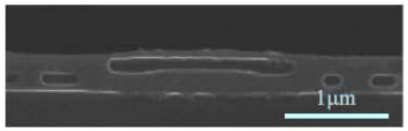
(a-4)mask thick 150nm , non ITOX,LTO



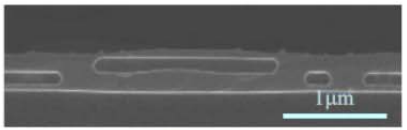
(b-4)mask thick 125nm, non ITOX,LTO



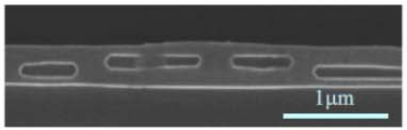
(c-4)mask thick 100nm, non ITOX,LTO



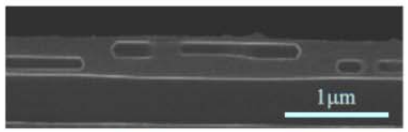
(a-5)mask thick 150nm , slight ITOX,LTO



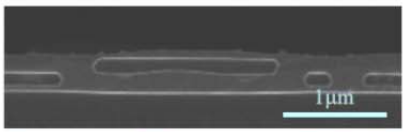
(b-5)mask thick 125nm, slight ITOX,LTO



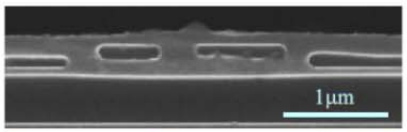
(c-5)mask thick 100nm, slight ITOX,LTO



(a-6)mask thick 150nm , normal ITOX,LTO

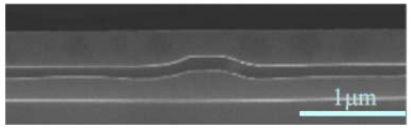


(b-6)mask thick 125nm, normal ITOX,LTO

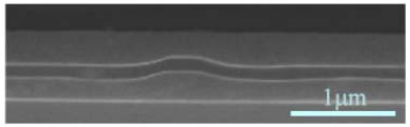


(c-6)mask thick 100nm, normal ITOX,LTO

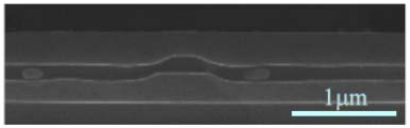
Appendix figure 1-4 cross sectional observation (mask width: 2.0μm)



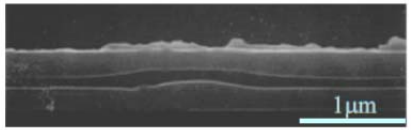
(a-1) 4.5×10^{17}/cm^2 ,non ITOX, without LTO



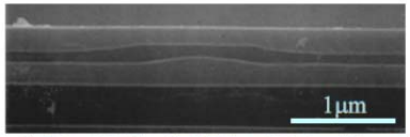
(b-1) 5.0×10^{17}/cm^2 ,non ITOX, without LTO



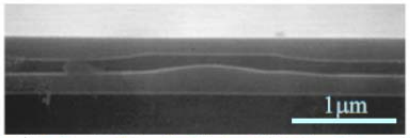
(c-1) 5.5×10^{17}/cm^2 ,non ITOX, without LTO



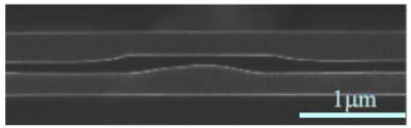
(a-2) 4.5×10^{17}/cm^2 ,Slight ITOX, without LTO



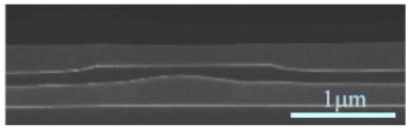
(b-2) 5.0×10^{17}/cm^2 ,Slight ITOX, without LTO



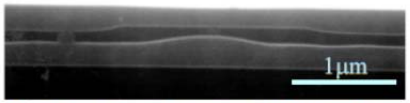
(c-2) 5.5×10^{17}/cm^2 ,Slight ITOX, without LTO



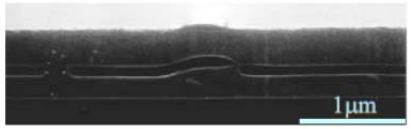
(a-3) 4.5×10^{17}/cm^2 ,normal ITOX, without LTO



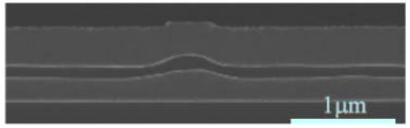
(b-3) 5.0×10^{17}/cm^2 ,normal ITOX, without LTO



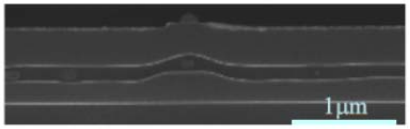
(c-3) 5.5×10^{17}/cm^2 ,normal ITOX, without LTO



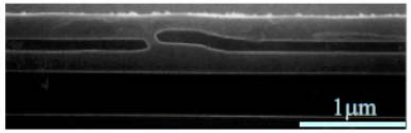
(a-4) 4.5×10^{17}/cm^2 ,non ITOX,LTO



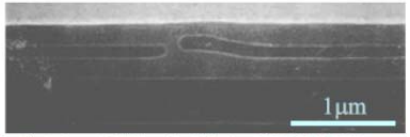
(b-4) 5.0×10^{17}/cm^2 ,non ITOX,LTO



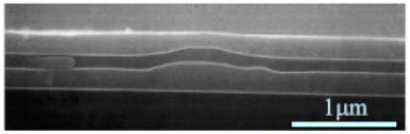
(c-4) 5.5×10^{17}/cm^2 ,non ITOX,LTO



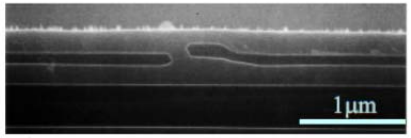
(a-5) 4.5×10^{17}/cm^2 ,Slight ITOX,LTO



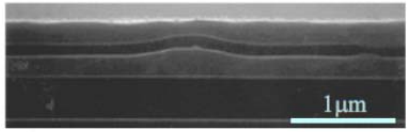
(b-5) 5.0×10^{17}/cm^2 ,Slight ITOX,LTO



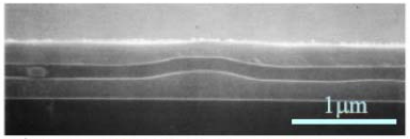
(c-5) 5.5×10^{17}/cm^2 ,Slight ITOX,LTO



(a-6) 4.5×10^{17}/cm^2 ,normal ITOX,LTO

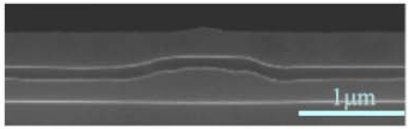


(b-6) 5.0×10^{17}/cm^2 ,normal ITOX,LTO

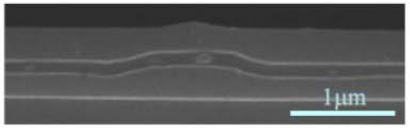


(c-6) 5.5×10^{17}/cm^2 ,normal ITOX,LTO

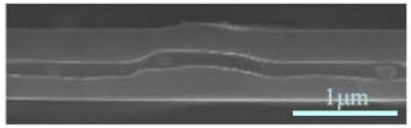
Appendix figure 2-1 cross sectional observation (mask width: 0.5μm)



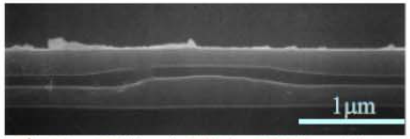
(a-1) 4.5×10^{17}/cm^2 ,non ITOX, without LTO



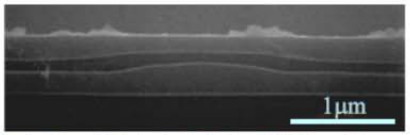
(b-1) 5.0×10^{17}/cm^2 ,non ITOX, without LTO



(c-1) 5.5×10^{17}/cm^2 ,non ITOX, without LTO

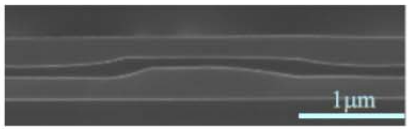


(a-2) 4.5×10^{17}/cm^2 ,Slight ITOX, without LTO

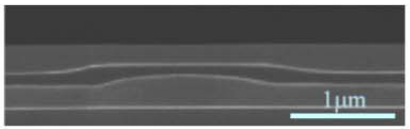


(b-2) 5.0×10^{17}/cm^2 ,Slight ITOX, without LTO

(c-2) 5.5×10^{17}/cm^2 ,Slight ITOX, without LTO



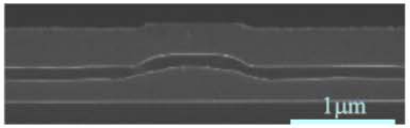
(a-3) 4.5×10^{17}/cm^2 ,normal ITOX, without LTO



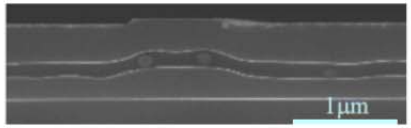
(b-3) 5.0×10^{17}/cm^2 ,normal ITOX, without LTO

(c-3) 5.5×10^{17}/cm^2 ,normal ITOX, without LTO

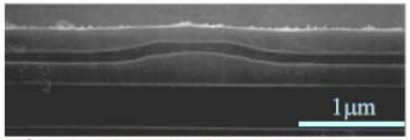
(a-4) 4.5×10^{17}/cm^2 ,non ITOX,LTO



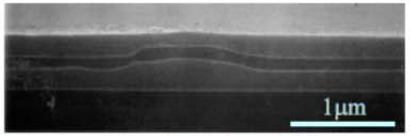
(b-4) 5.0×10^{17}/cm^2 ,non ITOX,LTO



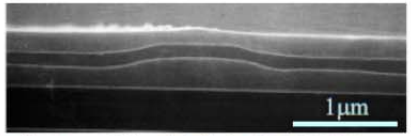
(c-4) 5.5×10^{17}/cm^2 ,non ITOX,LTO



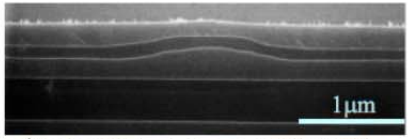
(a-5) 4.5×10^{17}/cm^2 ,Slight ITOX,LTO



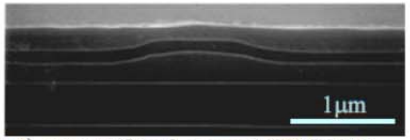
(b-5) 5.0×10^{17}/cm^2 ,Slight ITOX,LTO



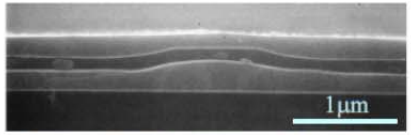
(c-5) 5.5×10^{17}/cm^2 ,Slight ITOX,LTO



(a-6) 4.5×10^{17}/cm^2 ,normal ITOX,LTO

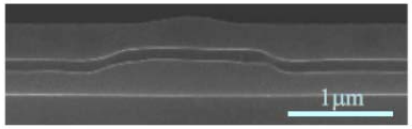


(b-6) 5.0×10^{17}/cm^2 ,normal ITOX,LTO

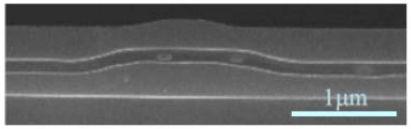


(c-6) 5.5×10^{17}/cm^2 ,normal ITOX,LTO

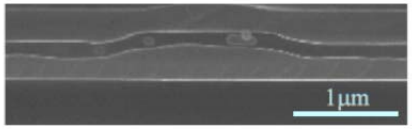
Appendix figure 2-2　cross sectional observation　(mask width: 1.0μm)



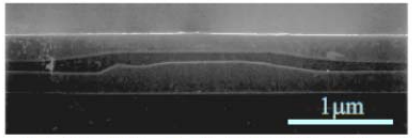
(a-1) 4.5×10^{17}/cm² ,non ITOX, without LTO



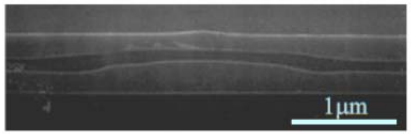
(b-1) 5.0×10^{17}/cm² ,non ITOX, without LTO



(c-1) 5.5×10^{17}/cm² ,non ITOX, without LTO

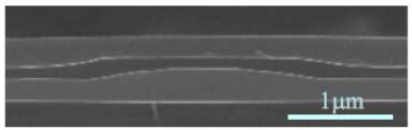


(a-2) 4.5×10^{17}/cm² ,Slight ITOX, without LTO

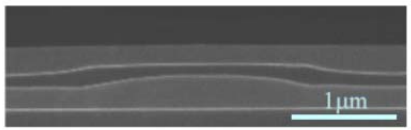


(b-2) 5.0×10^{17}/cm² ,Slight ITOX, without LTO

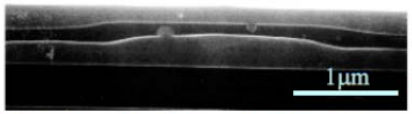
(c-2) 5.5×10^{17}/cm² ,Slight ITOX, without LTO



(a-3) 4.5×10^{17}/cm² ,normal ITOX, without LTO

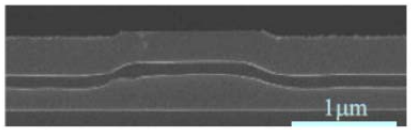


(b-3) 5.0×10^{17}/cm² ,normal ITOX, without LTO

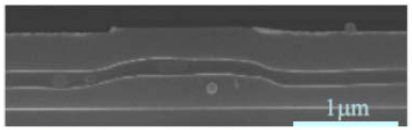


(c-3) 5.5×10^{17}/cm² ,normal ITOX, without LTO

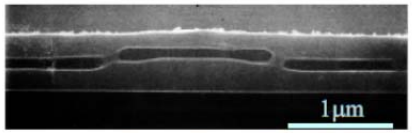
(a-4) 4.5×10^{17}/cm² ,non ITOX,LTO



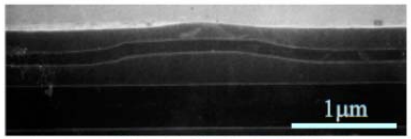
(b-4) 5.0×10^{17}/cm² ,non ITOX,LTO



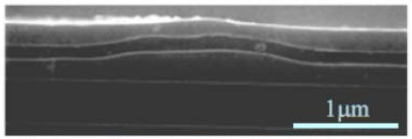
(c-4) 5.5×10^{17}/cm² ,non ITOX,LTO



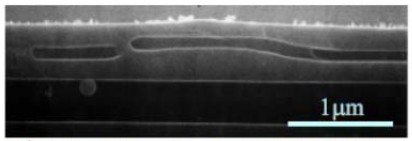
(a-5) 4.5×10^{17}/cm² ,Slight ITOX,LTO



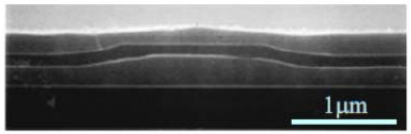
(b-5) 5.0×10^{17}/cm² ,Slight ITOX,LTO



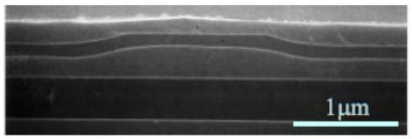
(c-5) 5.5×10^{17}/cm² ,Slight ITOX,LTO



(a-6) 4.5×10^{17}/cm² ,normal ITOX,LTO

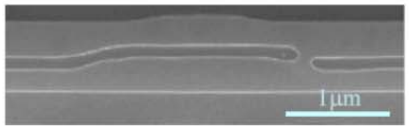


(b-6) 5.0×10^{17}/cm² ,normal ITOX,LTO

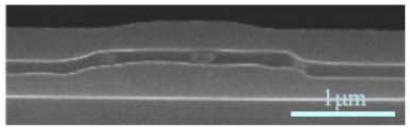


(c-6) 5.5×10^{17}/cm² ,normal ITOX,LTO

Appendix figure 2-3 cross sectional observation (mask width: 1.5μm)



(a-1) 4.5×10^{17}/cm^2 ,non ITOX, without LTO



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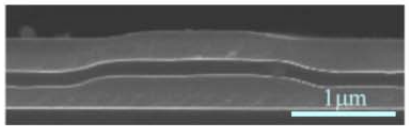

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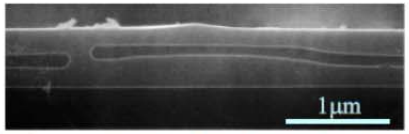

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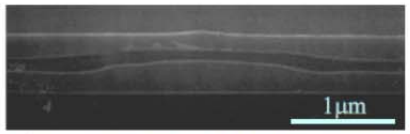

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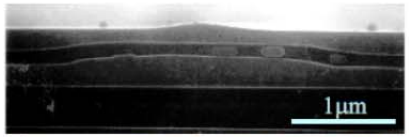

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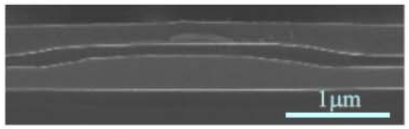
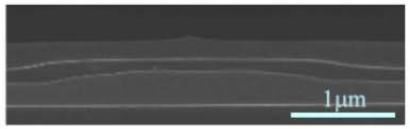


(a-3) 4.5×10^{17}/cm^2 ,normal ITOX, without LTO



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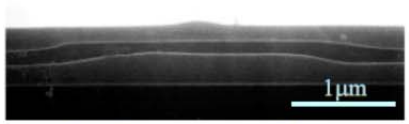
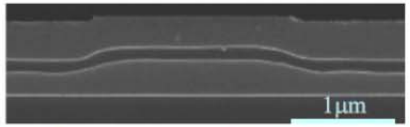


(c-3) 5.5×10^{17}/cm^2 ,normal ITOX, without LTO

(a-4) 4.5×10^{17}/cm^2 ,non ITOX,LTO



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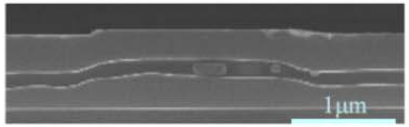

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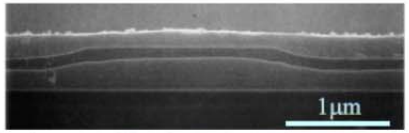

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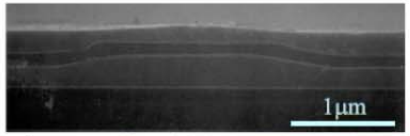

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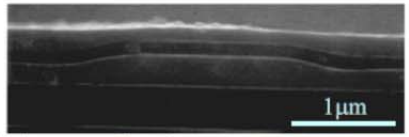

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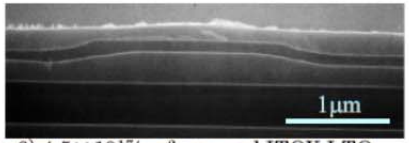
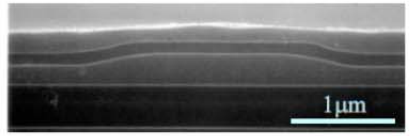


(a-6) 4.5×10^{17}/cm^2 ,normal ITOX,LTO



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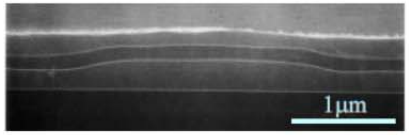

(c-6) 5.5×10^{17}/cm^2 ,normal ITOX,LTO

Appendix figure 2-4　cross sectional observation　(mask width: 2.0μm)

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